CLAIMS

1. A support for a semiconductor structure comprising a charge-trapping layer disposed on a base substrate, wherein the charge-trapping layer consists of a polycrystalline main layer and, interposed in the main layer or between the main layer and the base substrate, at least one intermediate layer composed of a silicon and carbon alloy or carbon, the intermediate layer having a resistivity greater than 1000 ohm·cm.

2. The support of claim 1, wherein the base substrate has a resistivity greater than 1000 ohm·cm.

3. The support of claim 2, wherein the charge-trapping layer has a thickness greater than 5 microns.

4. The support of claim 3, wherein the at least one intermediate layer comprises from one to ten intermediate layers.

5. The support of claim 4, wherein the at least one intermediate layer consists of a single intermediate layer composed of carbon between the main layer and the base substrate.

6. The support of claim 5, wherein the polycrystalline main layer consists of silicon grains with a size of between 100 nm and 1000 nm.

7. The support of claim 6, wherein each intermediate layer has a thickness of less than 10 nm.

8. The support of claim 1, further comprising an insulating layer on the charge-trapping layer.

9. The support of claim 1, wherein the at least one intermediate layer is composed of a silicon and carbon alloy having more than 5% carbon.

10. The support of claim 9, wherein the at least one intermediate layer comprises silicon carbide.

11. A semiconductor structure, comprising:
a support according to claim 1;
an insulating layer on the support; and
a useful layer on the insulating layer.

12. The semiconductor structure of claim 11, wherein the useful layer comprises at least one integrated device.

13. A method for manufacturing a semiconductor structure comprising the following steps:
providing a support according to claim 1; and
forming the semiconductor structure on the support.t

14. The method of claim 13, wherein forming the semiconductor structure on the support comprises transferring a useful layer onto the support.

15. The method of claim 14, wherein the useful layer comprises at least one integrated device.

16. The support of claim 1, wherein the charge-trapping layer has a thickness greater than 5 microns.

17. The support of claim 1, wherein the at least one intermediate layer comprises from one to ten intermediate layers.

18. The support of claim 1, wherein the at least one intermediate layer consists of a single intermediate layer composed of carbon between the main layer and the base substrate.

19. The support of claim 1, wherein the polycrystalline main layer consists of silicon grains with a size of between 100 nm and 1000 nm.

20. The support of claim 1, wherein each intermediate layer has a thickness of less than 10 nm.

21. The support of claim 1, wherein each intermediate layer is a polycrystalline or crystalline layer.