WHAT IS CLAIMED IS:

[Claim 1]. A semiconductor device, comprising:

a string of transistors stacked in a vertical direction over a substrate of the semiconductor device having a channel structure extending in the vertical direction, the string of transistors including ~~a~~ first, second and third substring of transistors that are arranged along ~~a~~ first, second and third portions of the channel structure, respectively, ~~a second substring arranged along a second portion of the channel structure, and a third substring of transistors that is arranged along a third portion of the channel structure,~~ the second substring of transistors being between the first substring of transistors and the third substring of transistors, wherein

gate structures of transistors in the first, second and third substring are separated by respective first, second and third insulating layers, ~~gate structures of transistors in~~ the second ~~substring are separated by second~~ insulating layers, ~~and gate structures of transistors in the third substring are separated by~~ have a higher etch rate than that of the third insulating layers, the string of transistors including a first discontinuity between critical dimensions (CDs) of the first and second portions of channel structure at a boundary between the first and second portions of the channel structure and a secondary discontinuity between CDs of the second and third portions of the channel structure and

~~a volumetric mass density~~ of the first discontinuity and the second discontinuity are less than a threshold that is between 0.05 and 0.15~~insulating layers is lower than a volumetric mass density of the third insulating layers~~.

~~2. The semiconductor device according to claim 1, wherein the volumetric mass density of the second insulating layers is lower than a volumetric mass density of the first insulating layers.~~

~~3. The semiconductor device according to claim 2, wherein the volumetric mass density of the first insulating layers is equal to the volumetric mass density of the third insulating layers.~~

~~4. The semiconductor device according to claim 1, wherein an etch rate of the second insulating layers is higher than an etch rate of the third insulating layers.~~

~~5. The semiconductor device according to claim 1, wherein the second insulating layers are silicon oxide formed by a high density plasma chemical vapor deposition and the third insulating layers are silicon oxide formed based on tetraethoxysilane.~~

~~6. The semiconductor device according to claim 1, wherein a material composition of the second insulating layers is different from a material composition of the third insulating layers.~~

[Claim 2~~7~~]. The semiconductor device according to claim 1, wherein ~~a~~ the first discontinuity between ~~a~~ the ~~critical dimension (~~CD~~)~~ at a bottom side of the second portion of the channel structure and ~~a~~ the CD at a top side of the first portion of the channel structure is less than a threshold.

[Claim 3~~8~~]. The semiconductor device according to claim ~~7~~2, wherein ~~a~~the second discontinuity between ~~a~~ the CD at a bottom side of the third portion of the channel structure and ~~a~~ the CD at a top side of the second portion of the channel structure is less than the threshold.

[Claim 4]. The semiconductor device according to claim 1, wherein a volumetric mass density of the second insulating layers is lower than that of the third insulating layers.

~~9. The semiconductor device according to claim 1, wherein a ratio of a number of transistors in the second substring over a sum of the number of transistors in the second substring and a number of transistors in the third substring is between 10 and 30%.~~

~~10. A semiconductor device, comprising:~~

~~a string of transistors stacked in a vertical direction over a substrate of the semiconductor device having a channel structure extending in the vertical direction, the string of transistors including a first substring of transistors arranged along a first portion of the channel structure, a second substring of transistors arranged along a second portion of the channel structure, and a third substring of transistors arranged along a third portion of the channel structure, the second substring of transistors being between the first substring of transistors and the third substring of transistors, wherein~~

~~the first portion of the channel structure has a tapered cylindrical shape, a critical dimension (CD) at a bottom side of the first portion being less than a CD at a top side of the first portion,~~

~~a CD in a middle of the second portion of the channel structure is larger than the CD at the bottom side of the first portion and a CD at a bottom side of the third portion, and~~

~~the third portion of the channel structure has a tapered cylindrical shape, the CD at the bottom side of the third portion being less than a CD at a top side of the third portion.~~

~~11. The semiconductor device according to claim 10, wherein a CD at a top side of the second portion of the channel structure is larger than the CD at the bottom side of the third portion.~~

~~12. The semiconductor device according to claim 10, wherein a CD at a bottom side of the second portion of the channel structure is larger than the CD at the bottom side of the first portion.~~

~~13. The semiconductor device according to claim 10, wherein~~

~~gate structures of transistors in the first substring are separated by first insulating layers, gate structures of transistors in the second substring are separated by second insulating layers, and gate structures of transistors in the third substring are separated by third insulating layers, and~~

~~a volumetric mass density of the second insulating layers is lower than a volumetric mass density of the third insulating layers.~~

[Claim ~~14~~5]. The semiconductor device according to claim 1~~3~~, wherein ~~the~~ a volumetric mass density of the second insulating layers is lower than a volumetric mass density of the first insulating layers.

~~15. The semiconductor device according to claim 14, wherein the volumetric mass density of the first insulating layers is equal to the volumetric mass density of the third insulating layers.~~

[Claim 6~~16~~]. The semiconductor device according to claim ~~13~~5, wherein the second insulating layers are silicon oxide formed by a high density plasma chemical vapor deposition and the third insulating layers are silicon oxide formed based on tetraethoxysilane.

[Claim 7~~17~~]. The semiconductor device according to claim ~~13~~1, wherein a material composition of the second insulating layers is different from a material composition of the third insulating layers.

[Claim 8~~18~~]. The semiconductor device according to claim 1~~0~~, wherein a ratio of a number of transistors in the second substring over a sum of the number of transistors in the second substring and a number of transistors in the third substring is between 10 and 30%.

[Claim 9]. The semiconductor device according to claim 1, wherein the first insulating layers and the third insulating layers have an identical etch rate.

~~19. The semiconductor device according to claim 10, wherein a discontinuity between a CD at a bottom side of the second portion of the channel structure and the CD at the top side of the first portion of the channel structure is less than a threshold.~~

~~20. The semiconductor device according to claim 19, wherein a discontinuity between the CD at the bottom side of the third portion of the channel structure and a CD at a top side of the second portion of the channel structure is less than the threshold.~~