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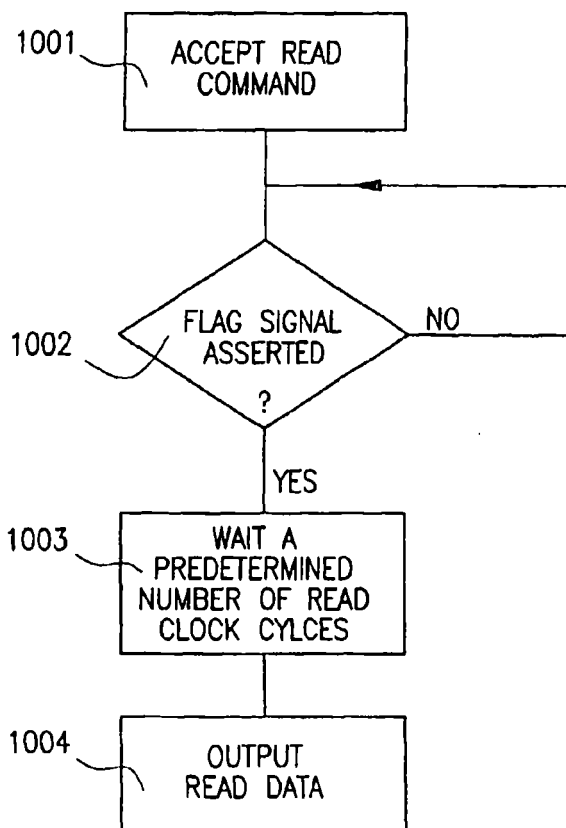
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(54) Title: A METHOD OF SYNCHRONIZING READ TIMING IN A HIGH SPEED MEMORY SYSTEM



(57) Abstract: The read latency of a plurality of memory devices in a high speed synchronous memory subsystem is equalized through the use of at least one flag signal. The flag signal has equivalent signal propagation characteristics read clock signal, thereby automatically compensating for the effect of signal propagation. After detecting the flag signal, a memory device will begin outputting data associated with a previously received read command in a predetermined number of clock cycles. For each of the flag signal, the memory controller, at system initialization, determines the required delay between issuing a read command and issuing the flag signal to equalize the system read latencies. The delay(s) are then applied to read transactions during regular operation of the memory system.

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