Title : Self-Aligned Unlanded Via Metallization

Abstract of the Invention

A multilevel interconnect is formed on an insulating layer over a semiconductor substrate by forming depressions such as trenches or grooves in the surface of the insulating layer. Metal wiring lines are formed by blanket depositing a layer of metal, filling the depressions on the surface of the insulating layer, and then chemical mechanical polishing the device to planarize the surface of the metal layer and the insulating layer, thereby forming a pattern of first level wiring lines. An etch stop layer of a material different from the insulating layer is deposited over the first level wiring lines and over the insulating layer. A layer of dielectric material, different from the layer of etch stop material, is deposited over the etch stop layer. A via is formed through the layer of dielectric material and the etch stop layer is removed from within the via. Next, a glue or adhesion layer is deposited within the via, a tungsten plug is formed within the via, and then a second level wiring line is formed in contact with the tungsten plug. This method avoids a poison via problem, thereby forming interconnects more reliably having low resistance levels.

(Fig. 11)