

Abstract

A semiconductor device has a first interconnect structure with an opening in the first interconnect structure. A PIC is disposed over the first interconnect structure with a photonic region aligned with the opening in the first interconnect structure. A plurality of conductive vias is formed at least partially through the PIC. An interconnect component having a plurality of conductive vias is disposed over the first interconnect structure. A plurality of bumps can be formed over the first interconnect structure. A second interconnect structure is disposed over the PIC and interconnect component. A protective layer is disposed within the opening over the photonic region. An electrical component is disposed over the second interconnect structure. The protective layer can have a dam formed over the PIC and an epoxy material disposed within the dam over the photonic region. Alternatively, the protective layer has an epoxy material disposed over the photonic region.

(Fig.7j)