

PID FILTER CIRCUIT AND FIFO CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to a filter circuit for executing a filtering in order to sample a required packet out of a data stream in which a time division transmission is implemented by a plurality of packets. More to particularly this invention relates to a filter circuit for discriminating the packet by PID (packet identifier) incorporated in the packet, and to an FIFO (first-in first-out) memory as being suitable for use in this filter circuit.

Description of the Prior Art

There is a method for transmitting a plurality of data by only one data stream. This method is to transmit packets through the time-division system while dividing data into unit called as the packet. In this case, there is added a packet identifier (PID) to respective packets in order to denote kinds of packet in terms of respective packets or which data corresponds to which packet. In many cases, the PID is included in the packet concerned. The receiving side of the data discriminates the PID of respective packets, before determining whether or not the packet is to be sampled in answer to the kind and so forth in connection with the packet being discriminated previously.

At the present time, there is widely used a procedure so called MPEG 2 (Moving Picture Experts Group 2) by way of a coding procedure for compression or transmission of image (or voice) data. In this MPEG 2, some kinds of packets are used. For instance, TS (Transport Stream) packet is a packet with fixed length of 188 bytes as shown in Fig. 1. There is allocated 13 bits from the twelfth bit from the top by way of the PID.

In some cases, there is not fixed the position of the PID in a data

transmission protocol or a data transmission system. In the packet shown in Fig. 2, the position of the PID is variable within the packet. However, as being a substitute of this state, there is stored the data (pointer for the PID) of denoting what position the PID exists, in the predetermined position of the packet. In this case as shown in Fig. 2, there is stored the pointer of the PID at the top of the packet.

In the system implementing transmission of the packet, the receiving side implements a judgement whether or not the transmitted packet is to be the treating object, before the receiving side is to sample only necessary packet. There is used the PID included in the transmitted packet for this judgement sake. Then, there is used a PID filter circuit in order to sample only the packet with the required PID.

Fig. 3 is a block diagram showing one example of configuration of the conventional PID filter circuit. Here, there is described the case where a length of the PID is the corresponding length of three words as being included within the packet.

There is provided flip-flops (FF) 61 to 63 in order to delay the input data by corresponding length of three words. An output side of the flip-flop 63 of the last stage is provided with an FIFO (First-in First-out) memory 60 for implementing the first-in first-out operation of the data. Further, the flip-flops 61 to 63 are provided with respective comparators 64 to 66 in order to compare the input for the flip-flop with the data predetermined beforehand. The output of comparison result of the respective comparators 64 to 66 is inputted to an AND gate 67 with three-input, thus there is controlled a write of the data for the FIFO memory 60 by the output of the AND gate 67.

There is described operation of this PID filter circuit as follows:

Since the respective flip-flops 61 to 63 permit the input data to

be delayed in answer to the corresponding length of one word, the comparator 64 implements a comparing operation in terms of the data with the corresponding length of present one word, the comparator 65 implements the comparing operation in terms of the data with the corresponding length of one word in front of the present one, and the comparator 66 implements the comparing operation in terms of the data with the corresponding length of one word in front of the present one by two words. For that reason, there is compared the data of continuous three words simultaneously by the flip-flops 61 to 63 and the comparators 64 to 66. Then, when the PID within the input packet agrees with the PID established beforehand, thus the output of the AND gate 67 becomes "1", because there is supplied the PID which is established beforehand to the respective comparators 64 to 66 by way of reference data, so that there is written the input packet into the FIFO memory 60.

However, there is the following problem in this Prior Art.

Firstly, the problem is that the length of the PID is fixed, such PID is the filtering object. In the example shown in Fig. 3, there can be implemented only the comparison of corresponding length of three-word PID. When it is necessary to compare the corresponding length of five-words of PID, five flip-flops and five comparators are to be provided respectively. Furthermore, there can not be used simple AND gate for treating the comparison result on the comparator in order to cope with an unsettled length of the PID. It becomes necessary to prepare a complicated circuit for obtaining a conjunction in accordance with the condition.

Secondly, the problem is that the position of the PID within the packet data is fixed. In the example shown in Fig. 3, it is necessary to exist the PID at the top of the packet data, in order to take the packet as being object into the FIFO memory 60.

Here, for instance, if the PID exists at the position from the top of the packet data by the corresponding order of three words, it is necessary to provide further two flip-flops in between the flip-flop 63 and the FIFO memory 60. Furthermore, in this case, it is always necessary to be included the PID in the determined position of the packet data, thus it can not be used the PID filter circuit when the position of the PID is unsettled.

As described above, there is the problem that in the conventional PID filter circuit, the length of the PID is fixed, and while it is necessary to be fixed the PID within the packet data.

SUMMARY OF THE INVENTION

In view of the foregoing, it is an object of the present invention to provide a PID filter circuit which is capable of coping with change of corresponding length of the PID or change of corresponding position of the PID within the packet data, and an FIFO memory being in use for this PID filter circuit.

According to the first aspect of the present invention, in order to achieve the above-mentioned object, there is provided a PID filter circuit for implementing a filtering of a packet data while discriminating a PID (Packet Identifier) within an input packet data, the PID filter circuit comprising a comparison value table for storing therein a comparison value beforehand, and a comparator for discriminating stored position of the PID within the input packet data, for taking out the comparison value successively from the comparison value table, and for comparing the value of the PID with the comparison value taken out in every one word by one word.

According to the second aspect of the present invention, there is provided a PID filter circuit, further comprising a FIFO (First-in, First-

out) memory for storing therein the input packet data in accordance with the method of first-in first-out, the FIFO memory not executing a read operation until the time when the input packet data is discriminated as being necessary one, while when the input packet data is discriminated as being unnecessary one, the PID filter circuit causes the input packet data to be cleared.

According to the third aspect of the present invention, there is provided a PID filter circuit wherein there is further provided with a first and a second FIFO (First-in First-out) memories for storing therein the input packet data, a first switch for inputting the input packet data to either one of the first and the second FIFO memories, and a second switch for selecting an output which is not selected by the first switch between the first and the second FIFO memories, when there is inputted the input packet data to either one FIFO memory between the first and the second FIFO memories, while there is outputted an output packet data from the other FIFO memory, when the input packet data stored in the one FIFO memory is the necessary one based on the result of comparing operation in the comparator, the PID filter circuit causes the output packet data to be outputted from the one FIFO memory while changing the first and the second switches.

According to the fourth aspect of the present invention, there is provided an FIFO circuit consisting of an FIFO memory for storing therein an input data in accordance with the method of first-in first-out, the FIFO memory comprising a dual port memory which stores therein the input data, and which is capable of executing a write operation and a read operation independently, a write pointer for maintaining a write address in terms of the dual port memory, a read pointer for maintaining a read address in terms of the dual port memory, a write control section for controlling a write operation in terms of the dual port memory, when there is implemented the write operation, it causes value of the write

pointer to be added by "1" (one), and when there is inputted a control signal denoting that the input data is unnecessary one, it causes value of the write pointer to be subtracted in accordance with data quantity of the input data, and a read control section for controlling a read operation in terms of the dual port memory in answer to a read demand from external side, when there is implemented the read operation, it causes value of the read pointer to be added by "1" (one), while when the input data is less than predetermined scale, there is not implemented the read operation regardless of the read demand.

As stated above, the PID filter circuit according to the invention stores the comparison value in the comparison value table beforehand, and the comparator reads out the comparison value from the comparison value table successively, thus executing the comparison with the PID section of the input packet data therebetween in every one word by one word. For that reason, even though when corresponding length of the word of the PID is long, it is suitable to enlarge only the comparison value table, and to prepare only one comparator.

In the configuration in which the FIFO memory is provided, it causes the input packet data to be maintained within the FIFO memory until the time when there can be discriminated whether or not the input packet data is necessary, when the input packet data is necessary one, it causes the input packet data to be used as it is, while when the input packet data is unnecessary one, there is superseded the input packet data in answer to the output of the comparator. For that reason, even though when the position of the PID within the packet data is unsettled, it is capable of being implemented surely the filtering of the packet without necessity of change of the circuit and so forth.

The above and further objects and novel features of the invention will be more fully understood from the following detailed description when the same is read in connection with the accompanying

drawings. It should be expressly understood, however, that the drawings are for purpose of illustration only and are not intended as a definition of the limits of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a view showing a configuration of TS (Transport Stream) packet in MPEG 2 (Moving Picture Experts Group 2);

Fig. 2 is a view showing one example of packet whose position of PID (Packet identifier) is variable;

Fig. 3 is a block diagram showing a configuration of the conventional PID filter circuit;

Fig. 4 is a block diagram showing a configuration of a PID filter circuit of a preferred embodiment of the invention;

Fig. 5 is a block diagram showing a configuration of FIFO memory; and

Fig. 6 is a block diagram showing a configuration of a PID filter circuit of another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A preferred embodiment of the present invention will be described in detail in accordance with the accompanying drawings. Fig. 4 is a block diagram showing a configuration of a PID filter circuit of a preferred embodiment of the invention, and Fig. 5 is a block diagram showing an internal configuration of FIFO memory.

The PID filter circuit shown in Fig. 4 is provided with an FIFO memory 11 which is a first-in first-out memory storing therein an input packet data to output it by way of an output packet data, a comparator 12 for comparing data of respective words of respective packets of the input packet data, and a comparison value table 13 for storing therein data (comparison value) which is used as reference data in comparing

operation in the comparator 12 beforehand. Here, the FIFO memory 11 stores therein the input packet data when there is a write demand from the external side, while the FIFO memory 11 outputs the output packet data when there is read demand from the external side, thus the operation of the FIFO memory 11 is controlled by an equality signal representing result of comparison in the comparator 12. Concretely, the FIFO memory 11 judges whether or not there is read out the input packet data actually in answer to the equality signal, further implementing a clearing of the data within the FIFO memory 11. The input packet data is written to the FIFO memory as it is. Further, since the comparison value table 13 is constituted by memory, the comparator 12 specifies a word order in connection with the PID in relation to the comparison value table 13, thus outputting the comparison value corresponding thereto.

Next, there is described an internal configuration of the FIFO memory 11 using Fig. 5. The FIFO memory 11 is provided with a memory 21 as being a dual port memory for storing therein the packet data actually. The memory 21 is capable of executing both of the write operation and the read operation independently, in particular, generally, implementing the write operation in accordance with the write demand from the external side. Further the FIFO memory 11 is provided with a write control section 22 for implementing write operation to the memory 21 in accordance with the write demand from the external side, a read control section 23 for implementing read operation from the memory 21 in accordance with read demand from the external side, a write pointer 24 for maintaining next write address in terms of the memory 21, a read pointer 25 for maintaining next read address in terms of the memory 21, and a subtracter 26 for calculating a difference between the write address maintained by the write pointer 24 and the read address maintained by the read pointer 25. The equality signal from the comparator 12 (Fig. 4) is inputted both to the write control section 22 and the read control section

23 by way of a control signal.

As described above, the memory 21 implements both of write operation in accordance with control of the write control section 22 and read operation in accordance with control of read control section 23. The write control section 22, when there is inputted the write demand from the external side, implements the write operation to the memory 21, thus increasing the value of the write pointer 24 by only 1 (one). Furthermore, when there is inputted the equality signal denoting that the PID is of disagreement and that the packet data is to be superseded, the write control section 22 implements annulment of the packet data by subtracting data quantity corresponding to the data written to the memory 21 from the value of the write pointer 24 in terms of the packet data. When the read demand is inputted from the external side, the read control section 23 implements the read operation to the memory 21 in answer both to a state of the equality signal and the output of the subtracter 26, thus there is increased the value of the read pointer 25 by one "1". Particularly, when the equality signal is not an equality signal representing the complete agreement and when output value of the subtracter 26 is less than the corresponding length of the packet, the read control section 23 does not execute the read operation regardless of existence of the read demand.

Next, there will be described operation of the PID filter circuit. A fundamental operation of the PID filter circuit is that when the input packet data is entered, it causes the packet data to be written to the FIFO memory 11 successively, simultaneously, the comparator 12 compares the data (comparison value) read out from the comparison value table 13 with the input packet data. The only one comparator 12 is in use regardless of word length of the PID or position thereof. When length of the PID is more than the corresponding length of two words, it causes the comparison value to be read from the comparison value table 13

successively, thus executing comparing operation successively. Furthermore, the FIFO memory 11 does not output the packet data at that time when the comparator 12 is in the comparing operation, even though there is the read demand from the external side. Moreover, in the result of comparison, when it is disagreement, causing the data to be superseded in terms of the data written to the FIFO memory 11 up to that time. On account of the above operation, the circuit shown in the present embodiment can operate by way of packet ID (PID) filter.

Hereinafter, there will be described operation of the PID filter circuit further in detail.

The input packet data possesses peculiar PID in every packet described above. For that reason, there is established the PID of necessary packet data out of packet data being transmitted, in the comparison value table 13 beforehand. When the PID section of the input data packet is transmitted, the comparator 12 reads out the PID established beforehand from the comparison value table 13, before comparing whether or not the PID section of the input data packet agrees with the PID established beforehand.

In general, the FIFO memory implements the read operation if the data is remained within the FIFO memory in response to the read demand from the external side, while the FIFO memory does not implement the read operation if the data is not remained within the FIFO memory. However, in this case of the PID circuit, there is not discriminated whether or not the input packet data is a packet data as being necessary in the midst that the comparator 12 compares the PID. For that reason, in this PID filter circuit, there is established that in response to the read demand, when there is the data with corresponding length of more than one packet within the FIFO memory 11, implementing the read operation, while when there is the data with corresponding length of less than one packet within the FIFO memory 11,

not implementing the read operation. The corresponding length of the data stored in the FIFO memory 11 is denoted by the output of the subtracter 26 because it is the difference between the next write address and the next read address. Further, in the result of comparison by the comparator 12, when the input packet data is not the packet data which is desired, at this time, there is superseded the packet data written in the FIFO memory 11. Moreover, the PID filter circuit permits the write of the packet data to be implemented unconditionally in relation to the FIFO memory 11. However, when there is discriminated that on the way of a packet data, the packet data is unnecessary in the result of comparison of the PID, at this time, there is implemented annulment of the packet data within the FIFO memory. Since it becomes unnecessary a section which does not arrive at the FIFO memory 11 yet of the packet data, it is also suitable that there is prohibited the following write operation in relation to the FIFO memory 11 of the packet data due to the equality signal.

Next, there will be described operation of the comparator 12. Firstly, the comparator 12 counts data number (for instance, byte number, octet number) from the top of the input packet data. When the position of the PID is unsettled and the position information (pointer) of the PID is included in the packet data, there is taken in the position information. When the position of the PID is fixed, there is established beforehand the position by for instance, the host CPU (not illustrated). In all cases, the comparator 12 counts the data number from the top of the input packet data to be detected the data of the PID section.

When the input data arrives at the position of the PID, the comparator 12 compares a value (here value of PID) of the input packet data with a value of the comparison value table 13. The comparator 12 obtains the comparison value while directing that it is the first word to the comparison value table 13, in relation to the first one word of the PID. Subsequently, the comparator 12 compares the above comparison value

with the first word of the PID, consecutively directing that it is the second word to the comparison value table 13 to obtain comparison value. Then, the comparator 12 compares the comparison value obtained with the second word. Thus the comparator 12 compares the PID in every corresponding length of one word successively as described above. Moreover, for instance, the host CPU permits the PID as being object to be written beforehand in the comparison value table 13. The comparator 12 compares the whole data of the comparison value table 13 with the PID within the input packet data. When only there agrees with any data, namely, when only the PID agrees therewith completely, thus communicating this state to the FIFO memory 11. Practically, the equality signal outputted from the comparator 12 represents that it is in the midst of comparing operation (it is included waiting period during when the input packet data does not arrive at the PID yet), or that the PID agrees therewith completely, or that the PID disagrees therewith.

Next, there will be described operation in the FIFO memory 11 using Fig. 5.

When there is the write demand in terms of the memory 21 as being dual port memory within the FIFO memory 11, the write control section 22 causes the write operation to be implemented in terms of the memory 21. At this time, there is referred to the write pointer 24 as the write address, after completion of the write operation, there is increased the value of the write pointer 24 by "1" (one) in accordance with the instruction of the write control section 22. There is operated the read operation in accordance with the read demand from the external side similar to the write operation. Similarly, when there is the read demand, the read control section 23 implements the read operation in relation to the memory 21. At this time, there is referred to the read pointer 25 as the read address, after completion of the read operation, there is increased the value of the read pointer 25 by "1" (one) in accordance with

the instruction of the read control section 23. Here, there is denoted quantity of the data stored in the memory 21 as being the difference between the value of write pointer 24 and the value of read pointer 25. When the value of the write pointer 24 equals to the value of the read pointer 25, there is stored the data in the memory 21, consequently, the read control section 23 does not reply to the read demand.

When the comparator 12 (Fig. 4) is in the comparing operation, the input packet data at this time can not be discriminated whether or not it is the required packet data. For that reason, in the state of comparing operation, there is implemented the write operation to the memory 11, however, when the difference between the write pointer 24 and the read pointer 25 is less than the corresponding length of packet, the read control section 23 does not reply the read demand, thus there is not implemented the read operation. After the comparison is terminated, when the data is the desired data (packet data in which the PID agrees therewith completely), the read control section 23 reply to the read demand. To the contrary, when the data is not the desired data (in the case where packet data in which the PID disagrees therewith exists), there is superseded the data written in the memory 21. The annulment of the data is realized such that there is subtracted corresponding number of the data number written to the memory 21 from the value of the write pointer 24. Moreover, concerning certain input packet data, it can be thought that it is the packet on the way of inputting, at the time of annulment. When there is intended to prevent further storing of the data into the FIFO memory 11 without superseding further data, it is suitable to prepare the configuration such that the write control section 22 does not execute the write operation when such the equality signal is inputted.

In the PID filter circuit, the comparator 12 counts the corresponding length of the data from the top of the packet data to be implemented the comparing operation. The comparator 12 remains the

packet data within the FIFO memory 11 until the time when there can be judged whether or not the packet data is necessary. There is used the data as it is if necessary, while there is superseded the data if unnecessary. Therefore, even though position of the PID within the packet data is unsettled, it is capable of implementing surely the packet filtering without changing circuit. Furthermore, since there is implemented the comparison successively in the comparator 12 while reading out the comparison value from the comparison value table 13, there is implement the comparison by only one comparator, even though word length of the PID becomes long, it is resolved by the fact that the comparison value table 13 is enlarged. Even though word length of the PID becomes long, there is scarcely changed circuit scale.

Fig. 6 is a block diagram showing a configuration of a PID filter circuit according to another embodiment of the present invention. The PID filter circuit shown in Fig. 6 is compared with the PID filter circuit shown in Fig. 4. The PID filter circuit shown in Fig. 6 is provided with two FIFO memories 11A, and 11B which FIFO memories are controlled by the equality signal from the comparator 12 and to which the input packet data is inputted, a switch 14 for allocating the input packet data to either one of the FIFO memories 11A, and 11B, and a switch 15 for selecting either one of the FIFO memories 11A, and 11B. In this connection the PID filter circuit shown in Fig. 6 differs from the PID filter circuit shown in Fig. 4. The switches 14 and 15 are interlocked so as to select different FIFO memories mutually, and are controlled by the equality signal.

In this PID filter circuit, when the switch 14 selects the FIFO memory 11A, the input packet data is written in the FIFO memory 11A, simultaneously, the PID included therein is compared with the value of the comparison value table 13 by the comparator 12. During the time period, the output packet data is read out from the FIFO memory 11B, because the switch 15 selects the FIFO memory 11B. When the input

packet data written in the FIFO memory 11B is necessary packet data, it causes the switches 14, 15 to be reversed by the equality signal, thus permitting the data read out from the FIFO memory 11A to be outputted by way of the output packet data. When the input packet data written in the FIFO memory 11A is unnecessary packet data, there is superseded the data within the FIFO memory 11A. For that reason, even though the packet data is a packet data whose position of the PID is unsettled, it is capable of being selected the packet data.

As described above, according to the present invention, there is read out the comparison value from the comparison value table to be implemented the comparison of the comparison value with the input packet data, therefore, even though when the word length of the PID is long, it is capable of being implemented required operation by enlarging the comparison value table, thus there is the effect that it can be achieved by preparing only one comparator. For that reason, there occur the effect that even though the word length of the PID becomes long, there is scarcely changed the circuit scale.

Furthermore, according to the present invention, with respect to the input packet data, there is remained the packet data within the FIFO memory until the time when there can be discriminated whether or not the packet data is necessary. There is used the packet data as it is if necessary, while there is superseded the packet data if unnecessary. Therefore, even though position of the PID is unsettled within the packet data, there is the effect that it is capable of being implemented filtering of the packet surely without necessity of change of the circuit or the like.

While preferred embodiments of the invention have been described using specific terms, such description is for illustrative purpose only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of the following claims.

WHAT IS CLAIMED IS:

1. A PID (Packet Identifier) filter circuit for implementing filtering of a packet data while discriminating a PID (Packet Identifier) within an input packet data comprising:

a comparison value table for storing therein a comparison value beforehand; and

a comparator for discriminating stored position of said PID within said input packet data, for taking out said comparison value successively from said comparison value table, and for comparing the value of said PID with the comparison value taken out in every one word by one word.

2. A PID filter circuit as claimed in claim 1, further comprising a FIFO (First-in, First-out) memory for storing therein said input packet data by the method of first-in first-out, wherein said FIFO memory does not execute a read operation until the time when said input packet data is discriminated as being necessary one, while when said input packet data is discriminated as being unnecessary one, said PID filter circuit causes said input packet data to be cleared.

3. A PID filter circuit as claimed in claim 1, further comprising a FIFO (First-in, First-out) memory for storing therein said input packet data by the method of first-in first-out, wherein said FIFO memory does not execute a read operation although a read demand is inputted while said comparator executes comparing operation.

4. A PID filter circuit as claimed in claim 1, wherein there is further provided with a first and a second FIFO (First-in First-out) memories for storing therein said input packet data, a first switch for inputting said input packet data to either one of said first and said second

FIFO memories, and a second switch for selecting an output which is not selected by said first switch between said first and said second FIFO memories, when there is inputted said input packet data to either one FIFO memory between said first and said second FIFO memories, while there is outputted an output packet data from the other FIFO memory, when the input packet data stored in said one FIFO memory is the necessary one based on the result of comparing operation in said comparator, said PID filter circuit causes the output packet data to be outputted from said one FIFO memory while changing said first and said second switches.

5. A PID filter circuit as claimed in claim 2, wherein said FIFO memory comprises:

- a dual port memory which stores therein said input packet data, and which is capable of executing a write operation and a read operation independently;

- a write pointer for maintaining a write address in terms of said dual port memory;

- a read pointer for maintaining a read address in terms of said dual port memory;

- a write control section for controlling said write operation in terms of said dual port memory, when said write operation is implemented, it causes value of said write pointer to be added by "1" (one), and when there is discriminated that said input packet data is unnecessary one based on the result of comparing operation through said comparator, it causes value of said write pointer to be subtracted in accordance with data quantity of said input packet data; and

- a read control section for controlling a read operation in terms of said dual port memory in accordance with a read demand from external side, when there is implemented a read operation, it causes value of said

read pointer to be added by "1" (one), while when data quantity within said dual port memory is less than corresponding length of a packet of said input packet data, there is not implemented said read operation regardless of said read demand.

6. A PID filter circuit as claimed in claim 5, wherein there is provided with a subtracter for calculating difference between value of said write pointer and value of said read pointer to output it to said read control section as being data quantity within said dual port memory.

7. An FIFO circuit consisting of an FIFO memory for storing therein an input data in accordance with method of first-in first-out, said FIFO memory comprising:

- a dual port memory which stores therein said input data, and which is capable of executing a write operation and a read operation independently;

- a write pointer for maintaining a write address in terms of said dual port memory;

- a read pointer for maintaining a read address in terms of said dual port memory;

- a write control section for controlling a write operation in terms of said dual port memory, when there is implemented the write operation, it causes value of said write pointer to be added by "1" (one), and when there is inputted a control signal denoting that said input data is unnecessary one, it causes value of said write pointer to be subtracted in accordance with data quantity of said input data; and

- a read control section for controlling a read operation in terms of said dual port memory in answer to a read demand from external side, when there is implemented the read operation, it causes value of said read pointer to be added by "1" (one), while when said input data is less

than predetermined scale, there is not implemented the read operation regardless of said read demand.

8. An FIFO circuit as claimed in claim 7, wherein there is provided with a subtracter calculating difference between the value of said write pointer and the value of said read pointer, thus outputting it to said read control section as data quantity within said dual port memory.