CLAIMS

WHAT IS CLAIMED IS:

1. An antenna apparatus (10) comprising:

a radiating layer (20) comprising a plurality of antenna elements (22) forming an antenna array;

a semiconductor wafer (40) comprising a plurality of tiles (42) each having beamforming circuits (48); and

a multi-layer interposer (30) comprising:

a lower dielectric layer (31) adjacent to the wafer;

an upper dielectric layer (33) adjacent to the radiating layer;

a metal layer (37) between the lower and upper dielectric layers and comprising a plurality of conductive traces (35);

a plurality of first vias (72) extending through both the upper and lower dielectric layers and electrically coupling the beamforming circuits to the plurality of antenna elements; and

a plurality of second vias (82) extending between the beamforming circuits and the conductive traces to interconnect the plurality of tiles,

wherein each of the plurality of tiles has an identical circuit configuration formed through an identical reticle-generated image (91).

2. The antenna apparatus (10) of claim 1, wherein the wafer further comprises saw streets (55) separating the plurality of tiles from one another.

3. The antenna apparatus (10) of claim 1, wherein the plurality of first vias are each a signal via (72s) of a ground-signal-ground (GSG) via transition that further comprises a first ground via (72g1) on one side of the signal via and a second ground via (72g2) on another side of the signal via.

4. The antenna apparatus (10) of claim 3, wherein:

the multi-layer interposer (30) has a stripline construction comprising the first dielectric layer, the second dielectric layer, a lower ground plane (39) between the wafer and the lower dielectric layer, and an upper ground plane (36) between the upper dielectric layer and the radiating layer, the upper ground plane serving as a ground plane for the antenna elements;

wherein the first and second ground vias are respectively connected on one end to respective first and second ground contacts (51g1, 51g2) on the wafer and are each connected on an opposite end to the upper ground plane.

5. The antenna apparatus (10) of claim 4, wherein the second vias (82s) are each a signal via of a via transition that further comprises a ground via (82g1) connecting a third ground contact of the wafer to the upper ground plane and a ground-ground connection connecting a fourth ground contact of the wafer to the lower ground plane.

6. The antenna apparatus (10) of claim 1, wherein the plurality of conductive traces of the metal layer are part of a combiner/divider network (35) that divides a radio frequency (RF) transmit signal received at an input/output (I/O) connection point (P4) of the interposer into a plurality of divided RF transmit signals each routed to one or more of the beamforming circuits using a respective one of the second vias at a respective end point (35e) of the combiner/divider network.

7. The antenna apparatus (10) of claim 6, wherein the RF transmit signal is received at the I/O connection point from a connection point on the wafer, using a via of the plurality of second vias within the interposer.

8. The antenna apparatus (10) of claim 6, wherein:

each of the divided transmit signals is routed to a respective tile of the plurality of tiles at the respective end point of the combiner/divider network; and

the respective tile further comprises an on-wafer combiner/divider, electrically connected to the respective end point, that further divides the divided signal into at least

two further divided signals and routes each further divided signal to a respective one of the beamforming circuits of the respective tile.

9. The antenna apparatus (10) of claim 1, wherein the plurality of conductive traces form a combiner/divider network (35), and at least one of the plurality of tiles includes an intermediate amplifier that amplifies a transmit signal or a receive signal routed by the combiner/divider network, through a first via of the plurality of second vias within the interposer, from/to an intermediate point of the combiner/divider network and outputs the amplified transmit or receive signal back to the combiner/divider network through a second via of the plurality of second vias.

10. The antenna apparatus (10) of claim 1, wherein the plurality of conductive traces form a combiner/divider network (35), and each of the plurality of tiles includes an intermediate amplifier (65) connectable on an input side through a first via of the plurality of second vias within the interposer to a respective intermediate point of the combiner/divider network and an output side connectable through a second via of the plurality of second vias to another respective intermediate point of the combiner/divider network, each intermediate amplifier configured to selectively amplify a transmit signal or a receive signal routed by the combiner/divider network.

11. The antenna apparatus (10) of claim 1, wherein the plurality of conductive traces form a combiner/divider network (35) that combines a plurality of radio frequency (RF) receive signals received by the antenna elements and adjusted by the beamforming circuits into a combined RF receive signal output using a via of the plurality of second vias within the interposer to a connection point on the wafer.

12. The antenna apparatus (10) of claim 1, further comprising a plurality of solder bumps (59) each electrically connecting a respective one of the first vias or the second vias to the wafer.

13. The antenna apparatus (10) of claim 1, wherein the wafer is directly bonded to the multi-layer interposer.

14. The antenna apparatus (10) of claim 1, wherein the radiating layer comprises an air-dielectric material grown on the interposer and supporting the antenna elements.

15. The antenna apparatus of claim 1, wherein the antenna elements are patch antenna elements each driven by a probe feed (27) electrically coupled to one of the first vias.

16. An antenna apparatus (10) comprising:

a radiating layer (20) comprising a plurality of antenna elements (22) forming an antenna array;

a semiconductor wafer (40) comprising a plurality of radio frequency (RF) beamforming circuits (48) each having transistor regions internally formed within the semiconductor wafer, each beamforming circuit comprising at least one phase shifter (54) and at least one of a transmit path amplifier (52) and a receive path amplifier (52); and

a multi-layer interposer (30) comprising:

a lower dielectric layer (31) adjacent to the semiconductor wafer;

an upper dielectric layer (33) adjacent to the radiating layer;

a metal layer (37) between the lower and upper layers and comprising a plurality of conductive traces that form a combiner/divider network (35) that combines and/or divides signals between the plurality of RF beamforming circuits and an input/output connection point (P4) of the interposer;

a plurality of first vias (72) extending through both the upper and lower layers and electrically coupling the plurality of RF beamforming circuits to the plurality of antenna elements; and

a plurality of second vias (82) extending between the RF beamforming circuits and the conductive traces, some of the second vias interconnecting the

antenna elements with the combiner/divider network through the RF beamforming circuits;

wherein the wafer includes at least one intermediate amplifier (62) that amplifies a transmit signal or a receive signal routed through another one of the second vias from/to an intermediate point of the combiner/divider network and outputs the amplified transmit or receive signal back to the combiner/divider network through a further one of the second vias.

17. The antenna apparatus (10) of claim 16, wherein:

the multi-layer interposer has a stripline construction comprising the first dielectric layer, the second dielectric layer, a lower ground plane (39) between the wafer and the lower dielectric layer, and an upper ground plane (36) between the upper dielectric layer and the radiating layer, the upper ground plane serving as a ground plane for the antenna elements.

18. The antenna apparatus (10) of claim 16, wherein:

the combiner/divider network divides a transmit signal into a plurality of divided transmit signals at respective end points of the combiner/divider network;

each of the divided transmit signals is routed to the wafer at a respective one of the end points; and

the wafer further comprises a plurality of on-wafer combiner/dividers (49), each electrically connected respectively to one of the end points, that further divides the divided transmit signal into at least two further divided signals and routes each further divided signal to a respective one of the RF beamforming circuits.

19. The antenna apparatus (10) of claim 16, wherein each of the transmit path amplifier and the receive path amplifier is a millimeter wave amplifier.

20. The antenna apparatus (10) of claim 16, wherein the multi-layer interposer is comprised of quartz or fused silica.

21. A method of fabricating an antenna apparatus (10), comprising:

sequentially applying an identical reticle image (91) to each of a plurality of regions of a semiconductor wafer (40) to thereby form respective tiles (42) within each region, each tile comprising radio frequency (RF) beamforming circuits (48) having ion implanted transistor regions within the wafer and a metallization pattern on a surface of the wafer (S102);

attaching an interposer (30) to the wafer (S104, S106), the interposer comprising a lower dielectric layer adjacent to the wafer, an upper dielectric layer, a metal layer between the lower and upper dielectric layers and comprising a plurality of conductive traces, a plurality of first vias extending through both the upper and lower layers, and a plurality of second vias extending between a lower surface of the interposer and the metal layer to interconnect the plurality of tiles; and

attaching a radiating layer, comprising a plurality of antenna elements, to an upper surface of the interposer such that the antenna elements are electrically coupled to the RF beamforming circuits through the plurality of first vias (S108, S110).

22. The method of claim 21, wherein said attaching the radiating layer to an upper surface of the interposer comprises:

growing an air-dielectric material on the interposer (S108);

forming probe feed vias (27) within the grown air-dielectric material electrically connected at first ends thereof to respective ones of the first vias (S110); and

forming the antenna elements on or within the air-dielectric material electrically connected to opposite ends of the probe feed vias (S110).

23. The method of claim 21, wherein said attaching an interposer to the wafer comprises attaching a plurality of solder bumps (59) to the lower surface of the interposer and/or to the wafer and soldering electrical contacts (51) of each of the wafer and the interposer to opposite sides of the plurality of solder bumps.

24. The method of claim 21, wherein said attaching an interposer to the semiconductor wafer comprises directly attaching the lower surface of the interposer to a major surface (41) of the wafer using a direct bonding interface bonding method.