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(54) IMPROVEMENTS IN AND RELATING TO SEMICONDUCTOR INTEGRATED DEVICES

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor integrated devices and further relates to methods of manufacturing such a semiconductor device.

In a known semiconductor integrated device, such as a monolithic integrated circuit, a semiconductor layer provided on one side of a monocrystalline semiconductor substrate body is divided into islands which are separated from each other by an isolation zone, at least one circuit element being formed in such an island, said island being isolated from the substrate body by at least one $p-n$ junction.

Such a $p-n$ junction need not necessarily coincide with the original surface of the substrate body but may also be present in the semiconductor layer or in the substrate body, being formed, for example, by impurity diffusion or by other doping, for example, ion implantation. The doping to obtain such a $p-n$ junction may even be carried out prior to the provision of the semiconductor layer, so-called buried layers being formed. In expressions of the type "isolation relative to the substrate body" or "conductivity type of the substrate body", the material having the original conductivity is to be considered as the substrate body, for example, as it has remained below buried layers and/or redoped zones formed possibly at the substrate surface.

In one form of such a known semiconductor device, the semiconductor layer is provided

epitaxially on a substrate body of the opposite conductivity type. The isolation zone is generally obtained by separation diffusion to form isolation zones having a conductivity type opposite to the conductivity type of the epitaxial layer, said isolation zone adjoining the substrate body.

Another known example is constituted by the structures described by Murphy et al in "Proceedings I.E.E.E.", September, 1969, pp. 1523—1528. The substrate body and the semiconductor layer provided epitaxially thereon are of the same conductivity type. At its lower boundary the island has a buried layer of the opposite conductivity type and a laterally surrounding zone of the opposite conductivity type which adjoins the buried layer. The isolation zone consists of the epitaxial material of the original conductivity type and adjoins the substrate body.

These known structures suffer from drawbacks. For example, an isolation by means of a $p-n$ junction biased in the reverse direction has a certain leakage current, a certain breakdown voltage and a significant capacitance. Furthermore the possibility exists of stray transistor effects and leakage paths along the surface of the semiconductor layer to the isolation zone or between regions of juxtaposed islands by inversion at said surface. The low breakdown voltages and high capacitance leakage near the junction to an isolation zone were generally avoided by avoiding sharp $p-n$ junctions between highly doped zones. This was done, for example, by choosing at least one zone to be comparatively high-ohmic, for example, a zone of the comparatively high-ohmic epitaxially deposited material of the provided semiconductor layer. In order to avoid short-circuit connections by inversion, channel stopping diffusion zones were often used which had to be present at some dist-

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ance from the $p-n$ junction between isolation zone and island, for which extra space was required.

When several semiconductor zones for a semiconductor circuit element are provided in such an island, said zones should in many cases be connected electrically, either to connection conductors or to zones of other islands. For that purpose, deeper situated zones also had to be conducted locally to the surface, and generally a highly doped contact zone was also used at the surface, for which the required space should be reserved. According to a known method, said connections were produced *via* metal tracks which generally were vapour-deposited and provided on an insulating coating present on the semiconductor surface, which coating was provided with windows where the contact with the zones was effected. A pattern of conductors was preferably designed so that it was not necessary for the various metal tracks to cross each other, if possible. For this purpose, a metal track had often to be conveyed from one contact place to another via a considerable roundabout route. This again resulted in an increase of stray capacitances.

According to the invention, there is provided a semiconductor integrated device having a monocrystalline semiconductor substrate body and a silicon semiconductor layer provided on one side thereof and divided into islands which are separated from each other by an isolation zone, at least one circuit element being at least partly formed in such an island, said island being isolated from the substrate body by at least one $p-n$ junction, at least the upper part of the isolation zone being constituted by a silicon oxide insulation layer sunken in the semiconductor layer by local oxidation of the semiconductor layer, a semiconductor zone associated with the said island being connected in an electrically conductive manner to a zone associated with an adjacent island by means of a connection zone which is passed underneath the sunken oxide layer, is isolated from the substrate body and adjoins the zones associated with the two islands.

Thus, for example, when deep-situated zones of two semiconductor circuit elements are to be connected together electrically, for example the collectors of two transistors of the same type, a compact structure can be obtained without the danger of strong stray side effects. In the known formation of islands with isolation zones obtained exclusively by diffusion, and transistors arranged in various islands, the collectors could be connected *via* a metal track passed in an insulated manner over the isolation zone. However, sufficient space had to be allowed at the surface for highly doped

contacting zones which had to be far enough remote from the junction with the diffused isolation zones. Another possibility was the formation of both transistors in a common island in which the two base zones, each with emitter zones diffused therein, were provided in a common collector zone. Unfavourable stray transistor effects, thyristor effects, inversion shortcircuit and other undesirable effects could occur. However, in a device in accordance with the invention, both collector zones can be interconnected by a connection zone which adjoins the two zones, passes through the isolation zone, and extends underneath the sunken oxide layer which separates two islands for two transistors from each other.

The sunken oxide layer may be sunken over only a part of the thickness of the semiconductor layer, and the part of the isolation zone for the island separation below the sunken oxide layer may be formed differently. The two zones of the juxtaposed islands may be connected, for example, by a connection zone of the material of the provided semiconductor layer, such material having been deposited epitaxially on the semiconductor substrate body. This connection zone passes through the isolation zone between the two islands. The connection zone preferably is a buried layer. It may adjoin a buried layer below one of the islands or both islands, which latter buried layer or layers form the zone or zones to be connected or form part thereof. The assembly of the connected buried layers may be formed in one step as one buried layer. The said buried layer or buried layers should be isolated from the semiconductor substrate body and will therefore preferably be of a conductivity type opposite to that of the substrate. Since such a buried layer usually extends also in the original semiconductor substrate body, the sunken oxide layer may be sunken at least throughout the thickness of the provided semiconductor layer.

When the substrate body and the semiconductor zones are of mutually opposite conductivity types, the locally provided connection zone preferably is of the same conductivity type as that of the provided semiconductor layer. Since in that case a connection with zones of a further juxtaposed island may not be desirable, a buried layer is preferably applied along the lower side of the sunken oxide layer at least where it adjoins this further island, said buried layer then being of the same conductivity type as the substrate. In the case in which the sunken oxide layer is sunken to the surface of, or to just in the semiconductor substrate body, such a buried layer of the same conductivity type as the substrate body may be used as a channel interrupting zone. However, if the buried layer of the same con-

ductivity type as the substrate is present along the lower side of the sunken oxide layer adjoining at least several islands, then, at the area where the connection zone is to be produced, the said buried layer of the conductivity type of the substrate body is preferably not provided rather than over-doped.

In the case in which the substrate body and the semiconductor layer provided thereon are of the same conductivity type, the separation between island and substrate body is obtained by using a buried layer along the lower side of such an island, said buried layer being of a conductivity type opposite to that of the substrate body and of the epitaxial layer. This buried layer may then adjoin the isolation zone, in particular the oxide layer sunken in the semiconductor layer. The buried layers of various islands may be insulated from each other by a sufficient intermediate space at the area of the isolation zone. If desirable, however, said buried layers, according to a preferred embodiment, may be connected underneath the sunken oxide layer by means of a buried connection zone. This connection zone may form one assembly with the buried layers.

It is to be noted that in Patent Application 31840/71 (Serial No. 1,353,488) of the same priority date a semiconductor device has been proposed having a semiconductor substrate body and a semiconductor layer provided thereon, both of a first conductivity type, having therein an island-shaped region of the first conductivity type adjoining the surface of the layer, which region comprises at least one semiconductor circuit element and is fully bounded on its lower side by a buried layer of a second conductivity type opposite to the first conductivity type extending below the island. The lateral isolation is formed by an electrically insulating oxide layer pattern sunken in the semiconductor layer and surrounding the island, and a zone of the second conductivity type adjoining the semiconductor surface and the sunken oxide and which separates the sunken oxide from the island and adjoins the buried layer. Such an adjoining zone of the second conductivity type adjoining the surface and the sunken oxide may also be present in an adjacent island. In accordance with the present invention, such a buried layer and adjoining zone associated with one such island may be connected, *via* a connection zone of the second conductivity type below the sunken oxide layer, with such an adjoining zone and buried layer associated with an adjacent island.

In the present specification, the expression "sunken oxide layer" is to be understood to mean an oxide layer which, as regards its depth in the semiconductor, is

clearly distinguished from differences in height at the surface as a result of usual planar methods with diffusions and oxide maskings. In such usual planar methods, differences in height at the surface may occur of only a few tenths of a micron. The sunken oxide layer is a genetic insulation layer manufactured by the conversion of the semiconductor material.

In connection with its function as a part of the isolation zone, the sunken oxide layer should be sunken over a reasonable depth in the semiconductor. This is desirable not only to obtain improved isolation zones between the islands, but the sunken oxide insulation layer may also create a sufficient distance between the underlying semiconductor material and conductors which may pass over the oxide layer so that the capacitive coupling between them will be small. The sunken oxide layer preferably extends in the semiconductor over a depth of more than $0.5\ \mu$.

In one preferred form, the semiconductor device on the side of the epitaxial layer has a substantially flat surface. A substantially flat surface is to be understood to mean herein a flatness which is of the same order as is obtained with conventionally used planar methods. Oxide layers of at most $0.5\ \mu$ are used in conventionally used planar methods. If in the conventionally used planar methods thick, non-sunken oxide skins of, for example, $2\ \mu$ should be used to decrease the wiring capacity by capacitive coupling between conductive strips on the oxide and the underlying semiconductor material and if windows should be etched in such a thick oxide, for example to provide contacts, the drawback of such a thick oxide is that the etching of said windows is associated with considerable underetching, while a difference in height of $2\ \mu$ should be bridged with the conductive connection between a contact in the window and a supply conductor on the oxide.

By using sunken silicon oxide, obtained by local oxidation of silicon while using a masking on adjacent semiconductor parts, for example by means of silicon nitride, substantially flat junctions can be obtained while nevertheless very thick insulating material suitable for a low wiring capacity is used. The original thickness of the oxidised semiconductor material actually determines the thickness of the resulting oxide insulation layer. Taking into account the ultimate height of the insulation on the semiconductor beside the sunken oxide layer, the semiconductor surface may previously be given such a profile that after the formation of the sunken oxide layer the surface of said layer comes at approximately the same level as the semiconductor surface beside the sunken oxide layer. The thickness of silicon

oxide formed by oxidation of silicon is approximately twice the thickness of the original silicon converted to silicon oxide by the oxidation so that a considerable increase in volume takes place by the conversion. Thus, silicon material may be etched away at the area where the sunken oxide layer is to be provided, preferably by using as an etchant-mask the masking which is used to locally mask against the oxidation in the formation of the sunken oxide layer; thus at the area where the sunken oxide layer is to be formed the semiconductor surface becomes located at a lower level than the adjacent semiconductor surface, namely to such a depth that after the formation of the sunken oxide layer the surface of the sunken oxide layer, due to the increase in volume, becomes located at approximately the same level as the adjacent semiconductor surface or the insulation ultimately applied thereon. Small unevennesses can be formed adjacent the edge of the oxide layer which are of such a nature that they do not prevent metal conductors being provided over the isolation zone.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:—

Figures 1 to 4 are detailed diagrammatic cross-sectional views of successive stages in the manufacture of a semiconductor device having island structure;

Figures 5 to 8 are detailed diagrammatic cross-sectional views of successive stages in the manufacture of another semiconductor device having island structure, and

Figure 9 is a detailed diagrammatic cross-sectional view of a further semiconductor device having island structure.

Starting material for the arrangement of Figure 1 is as conventionally used in semiconductor technology and comprises a monocrystalline semiconductor substrate body 2 of *n*-type silicon having a resistivity of 1 Ohm cm. The body 2 has a thickness of 200 microns. An *n*-type silicon layer 3 is deposited epitaxially on the body 2, which layer 3 has a thickness of 3 microns and a resistivity of 0.1 Ohm cm. Between the layer 3 and substrate 2 there are present *p*-type buried layers 5 having a boron doping of 10^{18} atoms/cc. A layer 19 of silicon nitride, 0.15 micron thick, is provided on the layer 3 by heating in an atmosphere containing SiH_4 and NH_3 at a temperature of approximately 1000°C . By heating in an atmosphere containing SiH_4 , CO_2 and H_2 a layer of silicon oxide is provided on said layer 19. For all the details of the methods to be used for the provision of the silicon nitride and silicon oxide layers mentioned in this example, as well as for the masking and etching of said layers, reference is made

to Philips Research Reports, April, 1970, pp. 118—132, in which paper all the information necessary to those skilled in the art is given.

While using photoresist methods conventionally used in semiconductor technology, an annular opening is etched in said double layer of silicon nitride and silicon oxide, after which the said oxide layer is removed in a HF buffer solution, grooves 20, depth 0.8 micron (see Figure 1), being then etched in the layer 3 by etching at 2°C with a liquid consisting of 170 ccm. of 60% HNO_3 , 280 ccm. of smoking HNO_3 , 110 ccm. of 40% HF and 440 ccm. of glacial acetic acid. In general the grooves are provided above those parts of the junction between the substrate body 2 and the semiconductor 3 where an intermediate space is present between the buried layers 5, but locally a groove 20 is present above such a buried layer 5.

By oxidation in water vapour which is saturated at 95°C , the silicon surface in the grooves 20 (see Figure 2) is then oxidized at 1000°C during which the nitride layer 19 is also covered with a thin oxide layer 21 until an oxide pattern 8 is formed in the grooves 20, the upper surface of said pattern substantially coinciding with the interface between the layers 3 and 19.

A layer 22 of silicon nitride (see Figure 3) is then provided throughout the surface by means of the already mentioned methods, and this layer is coated with a layer 23 of silicon oxide. By using a photoresist method, the oxide layer 23 is locally etched away after which apertures 24 are etched in the nitride layer 22 while using the remaining parts of the layer 23 as a mask (see Figure 4). The first nitride layer 19 is maintained since it is covered with the oxide layer 21 which is substantially not attacked by the etchant (usually phosphoric acid) with which the nitride is etched away.

Gallium is then indiffused. This is carried out at 1050°C in argon using gallium-doped silicon powder as a source, for 15 minutes. The gallium diffuses through the oxide but is masked by the silicon nitride. As a result of this an approximately 0.7 micron thick *p*-type zone is obtained (see Figure 7) which adjoins the buried *p*-type layer 5 of which in this example the distance to the surface is approximately 2 microns. The grooves 20 are at least so wide that after the gallium diffusion the zones 9 which belong to juxtaposed islands 4 do not touch each other. Where an intermediate space is present between the buried layers 5, no detrimental stray transistor effect is thus formed between the zones with the intermediate part of the layer 3 below the sunken oxide insulation layer 8, so that an effective island separation is obtained.

Where, however, the buried layer 5 fully extends underneath the oxide 8, parts of said buried layer which extend below juxtaposed islands are connected by a part extending locally underneath the insulation layer 8. By means of zones 9 an assembly of interconnected zones belonging to different islands 4 and extending locally to the surface is obtained.

One or more zones for semiconductor circuit elements to be formed in the islands 4 can be provided in the resulting structure after removing the layers 19, 21, 22 and 23 by means of further oxidation, masking and diffusion. The buried layers may serve for insulation or form part of a semiconductor circuit element in which a through-connection to a zone of an adjacent island can be obtained and moreover connections to the surface can be obtained, for example, for providing a surface contact.

Instead of using a buried layer 5 extending underneath an oxide layer 8, zones 9 on either side of the oxide layer 8 may locally extend underneath the oxide over such a distance that a continuous zone is obtained.

The method described has been given only by way of example and the device described may also advantageously be manufactured according to various other methods, for example, that which is described in the copending Patent Application No. 31841/71 (Serial No. 1,353,489).

The semiconductor circuit elements, for example, transistors, diodes, resistors, $p-n-p$ elements, and so on, can be provided in known manner in the islands 4. Instead of in an island 4 one or more of these elements may also be present entirely or partly in the form of conductive layers, for example, metal layers, on the island-shaped region 4 or on the oxide layer 13. Furthermore it is not necessary for the region constituted by the buried layer 5 and the zones 9 to form part of the said circuit element although this is very desirable from a point of view of space saving.

It will be obvious that many modifications are possible. For example, the buried layer 5 can also be provided, if desirable, by ion implantation or epitaxially.

It is also possible to use, exclusively underneath the sunken oxide insulation layer, a buried layer of a conductivity type opposite to that of the epitaxial layer, which buried layer has expanded in the epitaxial layer from the substrate. At the area of the connection zone between two zones present in adjacent islands said layer may be interrupted. Such a case will hereinafter be described with reference to Figures 5 to 8.

Starting material is a monocrystalline semiconductor body 61 of p -type silicon in which by means of conventional planar methods arsenic-doped low-ohmic n -type

zones 62 and a boron-doped low-ohmic p -type zone 63 are formed. The zone 63 has the form of a network which, however, is interrupted locally. For the rest, the zone 63 encloses the zones 62 laterally. At the area of the interruption in the zone 63, the zone 62 is passed through the interruption. The parts of said zone 63 have a width, for example, of $3\ \mu$. The resulting stage is shown in Figure 5. As is usual in planar diffusion methods, an oxide layer 64 is present on the surface of the semiconductor body 61. This oxide layer is now removed in a conventional manner by means of hydrofluoric acid.

A high-ohmic n -type epitaxial layer 68 is then deposited on the silicon body 61, for example, in a thickness of $4\ \mu$. During said deposition the zones 62 and 63 which become buried layers, can expand into the epitaxial layer 68 by diffusion. In particular the buried layer 63 can expand more rapidly than the buried layer 62 since boron diffuses more rapidly than arsenic.

In known manner the surface of the epitaxial layer 68 is covered with a thin silicon nitride layer 65 and then with a silicon oxide layer 66. In this layer apertures are provided above the p -type buried zone 63, also in the form of a network, but now expanded above the interruption(s) in the network of the buried zone 63. The width of said apertures is at least $5\ \mu$. While using the nitride oxide masking 65, 66, grooves 67 are etched in the silicon in a depth of well over $1\ \mu$. The resulting stage is shown in Figure 6.

The oxide layer 66 is now removed by a conventional hydrofluoric acid etchant and the assembly is then subjected to an oxidizing treatment in steam of 1 atmosphere at 1000°C to form a sunken oxide insulation layer 70 consisting of silicon oxide, the silicon nitride masking 65 protecting the underlying silicon outside the grooves 67. The oxidation treatment is continued (approximately 16 hours) until a depth of approximately $2\ \mu$ is achieved, the formed oxide having also filled the original grooves 67 entirely. In the meantime the boron-doped p -type buried layer 63 has expanded further in the epitaxial layer. In this stage or after a subsequent thermal treatment it may adjoin the lower side of the sunken oxide insulation layer. The resulting stage is shown in Figure 7. The epitaxial layer 68 is now divided into islands which are separated from each other by means of isolation zones formed by the sunken oxide insulation layer 70 and the buried p -type layer 63. Locally, however, such an isolation zone below the sunken oxide insulation layer is interrupted for passing through an n -type conductive connection consisting of a part of the buried layer 62 and possibly a remainder present

above said layer of the original epitaxially deposited *n*-type material 68.

For example, by means of planar diffusion methods, circuit elements may then be formed in the islands in known manner, as the *n-p-n* transistor shown in Figure 8, in which the collector is formed by the epitaxial *n*-type material 78, the arsenic-doped buried layer 62, and the collector-contacting zone 77 formed during the emitter diffusion, the base is formed by the *p*-type zone 75 formed by diffusion of boron, and the emitter is formed by the *n*-type zone 76 formed by diffusion of phosphorus. The resulting stage is shown in Figure 8.

By means of the *n*-type buried layer 62, the collector zone belonging to the island 78 is through-connected to an *n*-type zone associated with an adjacent island via an interruption in the *p*-type buried layer 63 which together with the sunken oxide insulation layer 70 forms the isolation zone between the islands.

Since it had been ensured in the manufacture that the sunken oxide insulation layer was wider than the buried *p*-type layer 63, the distance between the buried layer 63 and the base zone 75 is maintained large notwithstanding the fact that the base layer 75 adjoins the sunken oxide insulation layer 70.

Also in the case of the device shown diagrammatically in Figure 8, the advantage is obtained that the upper side of the sunken oxide insulation layer 70 is present approximately at the same level as the adjacent surface of the epitaxial layer. In known manner, adjoining contacts in windows in thin insulation layers used on the island surface may be provided and supply conductors used which preferably extend over the sunken insulation layer 70 as much as possible.

In the case described in Figure 8 a thick epitaxial layer is used in which it is avoided, however, for the good formation of isolation zones, to use a proportionally thicker sunken oxide insulation layer. If desirable, the thickness of the epitaxial layer 68 may also be chosen to be smaller so that the sunken insulation layer 70 reaches at least to the junction between the substrate 61 and the provided semiconductor layer 68. Since the buried layer 62 extends in the original substrate, said layer can also produce locally below the sunken oxide insulation layer a conductive connection between two zones on either side of the isolation zone.

It is obvious that in the islands beside the island in which the transistor shown in Figure 8 is provided, other circuit elements, for example, other transistors, may also be provided.

In the embodiment shown in Figure 8 in which an *n*-type epitaxial layer is used on

a *p*-type substrate and an insulation layer which is partly sunken in said epitaxial layer, use is made of a highly doped buried layer of the *p*-type provided in the substrate, which layer has expanded to the lower side of the sunken insulation layer by diffusion. It is of course also possible, for example in the case of an epitaxial layer of the *n*-type on a substrate of the *p*-type and an oxide insulation layer sunken over part of the thickness of the epitaxial layer, to use a zone present on the lower side of the isolation zone in the epitaxial layer of the conductivity type of the substrate. This *p*-type zone present below the sunken oxide insulation layer may have expanded, for example, by diffusion to the *p-n* junction formed between the substrate and the epitaxial layer. It is also possible that said *p*-type zone adjoining the sunken oxide insulation layer has expanded to the depletion layer formed between the *p*-type substrate and the epitaxial layer.

The above example described with reference to Figures 5 to 8 related to a *p*-type semiconductor substrate body and an *n*-type epitaxial semiconductor layer. Of course, in a corresponding manner the starting material may be an *n*-type semiconductor substrate body and a *p*-type semiconductor layer in which the various zones and buried layers may also be chosen to be of correspondingly different conductivity type in a corresponding manner. In that case as an *n*-type doping material in silicon, for example, phosphorus, may be used as a doping for the buried layers 63 of Figure 8. Both boron and phosphorus have a very high solubility in silicon, while their diffusion properties do not differ much.

Figure 9 shows possibilities of island isolation in a device in accordance with the invention in the case in which a monocrystalline substrate body is used of the same conductivity type as the epitaxial layer provided thereon. The monocrystalline silicon substrate body 100 consists, for example, of *n*-type material having a resistivity of, for example, 1 ohm cm. An epitaxial layer 104 provided therein consists of silicon of the same conductivity type and approximately the same resistivity, while on the boundary of the substrate body and the epitaxial layer a number of buried layers 101, 102 and 103 of *p*-type silicon are provided which are separated from each other by a network of narrow zones 111 of the high-ohmic *n*-type material of the substrate and the epitaxial layer. The buried layers are doped, for example, with boron and have expanded from the boundary between the substrate and the epitaxial layer.

From the upper side of the epitaxial layer a sunken oxide insulation layer is provided as described above, the upper surface of which is approximately at the same level with

the upper side of the adjacent parts of the epitaxial layer. The sunken oxide layer 109 overlaps *inter alia* the *n*-type zones between the buried layers 101, 102 and 103. Furthermore, it is also provided locally according to intermediate strips from above, for example, to a central portion of the buried layer 102. In this manner the epitaxial layer 104 is divided into *n*-type islands 105, 106, 107 and 108 which are separated from the *n*-type substrate 100 by two *p-n* junctions and are separated from each other by isolation zones which partly consist of the sunken oxide insulation layer 109. For example, the islands 105 and 106 are separated from each other by the sunken oxide insulation layer 109, the parts facing each other of the buried layers 102 and 103, and the intermediate high-ohmic *n*-type zone 111, the islands 106 and 107 are separated from each other by the sunken oxide insulation layer 109 and the buried layer 102, and the islands 107 and 108 are separated from each other by the sunken oxide insulation layer 109, the end parts facing each other of the buried layers 101 and 102 and the intermediate high-ohmic *n*-type zone 111. Semiconductor circuit elements can be formed in known manner in the islands which are separated from each other. It is possible that such an underlying buried layer 102 serves as an isolation zone having two back-to-back *p-n* junctions. It is also possible that such a buried layer which actually is separated from the substrate by a *p-n* junction of the *n*-type material, forms a functional part of a circuit element to be provided, for example the collector of a *p-n-p* transistor. Since the layer 102 is provided below more than one island, it may also serve as a circuit-element through-connection, for example as a common, possibly floating, electrode of two circuit elements provided in the islands 106 and 107. Such a buried layer may also form a functional part of a circuit element and an isolation for another circuit element. Furthermore, in order to obtain islands of larger depth it is possible to use layers the upper side of which is situated deeper than the lower side of the sunken oxide insulation layer, narrow intermediate zones of the conductivity type of the buried layers producing a connection between the sunken oxide insulation layers and the buried layers in such manner that islands which are separated from each other are formed which, however, can locally have a larger depth than the sunken oxide insulation layer 109.

A structure of islands corresponding to Figure 9 may also be obtained by using a *p*-type substrate 100 on which *p*-type epitaxial material 104 is provided and in which *n*-type buried layers 101, 102 and 103 are used.

It is to be noted that many modifications

are possible within the scope of this invention. Semiconductor circuit elements having contacts of the Schottky type may also be used, while field effect transistors can be realized in known manner having a conducting path between "source" and "drain" to be cut-off by variation of the depletion layer of a *p-n* junction, in particular in the device shown in Figure 9. For example, in the island 107 a *p*-type zone 113 may be diffused-in which, with the buried layer 102, forms a gate for the current path from source 114 to drain 115 via the narrow gate zone 116 which can be cut-off by applying a sufficient reverse voltage at the gate electrode 113. It is also possible to use the narrowed part 116 of the high-ohmic *n*-type material as a resistor.

Many variations are possible within the scope of the present invention. In Figure 7, for example, two islands can be connected electrically, if desirable, solely via the epitaxial material 68 or solely via the buried *n*-type layer 62 with a local interruption of the *p*-type buried layer 63. If desirable, the sunken oxide insulation layer may also comprise extensions present in the islands, for example, as a substratum for wiring. The sunken oxide insulation layer may comprise widenings, for example, to serve as a substratum of a number of conductive strips or at the area where external supply conductors can be secured, for example, by soldering.

WHAT WE CLAIM IS:—

1. A semiconductor integrated device having a monocrystalline semiconductor substrate body and a silicon semiconductor layer provided on one side thereof and divided into islands which are separated from each other by an isolation zone, at least one circuit element being at least partly formed in such an island, said island being isolated from the substrate body by at least one *p-n* junction, at least the upper part of the isolation zone being constituted by a silicon oxide insulation layer sunken in the semiconductor layer by local oxidation of the semiconductor layer, a semiconductor zone associated with the said island being connected in an electrically conductive manner to a zone associated with an adjacent island by means of a connection zone which is passed underneath the sunken oxide layer, is isolated from the substrate body and adjoins the zones associated with the two islands.

2. A semiconductor device as claimed in Claim 1, in which the depth to which the sunken oxide layer is sunken in the semiconductor is more than 0.5 microns.

3. A semiconductor device as claimed in Claim 2, in which the difference in height at the surface between the sunken oxide layer and the adjacent semiconductor surface is at most 0.5 microns.

the upper side of the adjacent parts of the epitaxial layer. The sunken oxide layer 109 overlaps *inter alia* the *n*-type zones between the buried layers 101, 102 and 103. Furthermore, it is also provided locally according to intermediate strips from above, for example, to a central portion of the buried layer 102. In this manner the epitaxial layer 104 is divided into *n*-type islands 105, 106, 107 and 108 which are separated from the *n*-type substrate 100 by two *p-n* junctions and are separated from each other by isolation zones which partly consist of the sunken oxide insulation layer 109. For example, the islands 105 and 106 are separated from each other by the sunken oxide insulation layer 109, the parts facing each other of the buried layers 102 and 103, and the intermediate high-ohmic *n*-type zone 111, the islands 106 and 107 are separated from each other by the sunken oxide insulation layer 109 and the buried layer 102, and the islands 107 and 108 are separated from each other by the sunken oxide insulation layer 109, the end parts facing each other of the buried layers 101 and 102 and the intermediate high-ohmic *n*-type zone 111. Semiconductor circuit elements can be formed in known manner in the islands which are separated from each other. It is possible that such an underlying buried layer 102 serves as an isolation zone having two back-to-back *p-n* junctions. It is also possible that such a buried layer which actually is separated from the substrate by a *p-n* junction of the *n*-type material, forms a functional part of a circuit element to be provided, for example the collector of a *p-n-p* transistor. Since the layer 102 is provided below more than one island, it may also serve as a circuit-element through-connection, for example as a common, possibly floating, electrode of two circuit elements provided in the islands 106 and 107. Such a buried layer may also form a functional part of a circuit element and an isolation for another circuit element. Furthermore, in order to obtain islands of larger depth it is possible to use layers the upper side of which is situated deeper than the lower side of the sunken oxide insulation layer, narrow intermediate zones of the conductivity type of the buried layers producing a connection between the sunken oxide insulation layers and the buried layers in such manner that islands which are separated from each other are formed which, however, can locally have a larger depth than the sunken oxide insulation layer 109.

A structure of islands corresponding to Figure 9 may also be obtained by using a *p*-type substrate 100 on which *p*-type epitaxial material 104 is provided and in which *n*-type buried layers 101, 102 and 103 are used.

It is to be noted that many modifications

are possible within the scope of this invention. Semiconductor circuit elements having contacts of the Schottky type may also be used, while field effect transistors can be realized in known manner having a conducting path between "source" and "drain" to be cut-off by variation of the depletion layer of a *p-n* junction, in particular in the device shown in Figure 9. For example, in the island 107 a *p*-type zone 113 may be diffused-in which, with the buried layer 102, forms a gate for the current path from source 114 to drain 115 via the narrow gate zone 116 which can be cut-off by applying a sufficient reverse voltage at the gate electrode 113. It is also possible to use the narrowed part 116 of the high-ohmic *n*-type material as a resistor.

Many variations are possible within the scope of the present invention. In Figure 7, for example, two islands can be connected electrically, if desirable, solely via the epitaxial material 68 or solely via the buried *n*-type layer 62 with a local interruption of the *p*-type buried layer 63. If desirable, the sunken oxide insulation layer may also comprise extensions present in the islands, for example, as a substratum for wiring. The sunken oxide insulation layer may comprise widenings, for example, to serve as a substratum of a number of conductive strips or at the area where external supply conductors can be secured, for example, by soldering.

WHAT WE CLAIM IS:—

1. A semiconductor integrated device having a monocrystalline semiconductor substrate body and a silicon semiconductor layer provided on one side thereof and divided into islands which are separated from each other by an isolation zone, at least one circuit element being at least partly formed in such an island, said island being isolated from the substrate body by at least one *p-n* junction, at least the upper part of the isolation zone being constituted by a silicon oxide insulation layer sunken in the semiconductor layer by local oxidation of the semiconductor layer, a semiconductor zone associated with the said island being connected in an electrically conductive manner to a zone associated with an adjacent island by means of a connection zone which is passed underneath the sunken oxide layer, is isolated from the substrate body and adjoins the zones associated with the two islands.

2. A semiconductor device as claimed in Claim 1, in which the depth to which the sunken oxide layer is sunken in the semiconductor is more than 0.5 microns.

3. A semiconductor device as claimed in Claim 2, in which the difference in height at the surface between the sunken oxide layer and the adjacent semiconductor surface is at most 0.5 microns.



4. A semiconductor device as claimed in any of the preceding Claims, in which the two zones are of the same conductivity type, and the conductive connection zone between the two zones is constituted by a buried layer of the said same conductivity type present below the sunken oxide layer.

5. A semiconductor device as claimed in Claim 4, in which at least parts of the two connected zones and the conductive connection zone therebetween together are constituted by a common buried layer.

6. A semiconductor device as claimed in Claim 4 or Claim 5, in which the buried layer is of a conductivity type opposite to that of the semiconductor substrate.

7. A semiconductor device as claimed in any of the preceding Claims, in which the isolation zone comprises a buried layer of the same conductivity type as the semiconductor substrate body present underneath the sunken oxide layer, which buried layer is interrupted at the area of the conductive connection zone which is of a conductivity type opposite to that of the substrate body.

8. A semiconductor device as claimed in any of the preceding Claims, in which the semiconductor substrate body and the semiconductor layer provided thereon are of opposite conductivity types and the locally provided conductive connection zone is of the same conductivity type as the provided semiconductor layer.

9. A semiconductor device as claimed in any of Claims 1 to 6, in which the semiconductor substrate body and the semiconductor layer provided thereon are of the same conductivity type, and along the lower side of each island a buried layer is used which separates the island from the sub-

strate, said buried layer being of a conductivity type opposite to that of the substrate body and the semiconductor layer, such a buried layer being locally connected to the buried layer of an adjacent island by the conductive connection zone.

10. A semiconductor device as claimed in Claim 9, in which the buried layer adjoins the sunken oxide layer.

11. A method of manufacturing a semiconductor device according to any of the preceding Claims.

12. A semiconductor integrated device substantially as herein described with reference to Figure 4 of the accompanying drawings.

13. A semiconductor integrated device substantially as herein described with reference to Figure 8 of the accompanying drawings.

14. A semiconductor integrated device substantially as herein described with reference to Figure 9 of the accompanying drawings.

15. A method of manufacturing a semiconductor device, substantially as herein described with reference to Figures 1 to 4 of the accompanying drawings.

16. A method of manufacturing a semiconductor device, substantially as herein described with reference to Figures 5 to 8 of the accompanying drawings.

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