

# **SPECIFICATION** **Electron-beam Programmable Semiconductor Device Structure**

This invention relates to electron-beam programmable semiconductor device structures and in particular to semiconductor device structures which include an electrically isolated conductor which is adapted to receive electric charge from an electron beam.

State of the art developments in semiconductor devices and particularly in high density arrays of semiconductor devices in integrated circuits include numerous examples where stored charge is used to control device operation. One such example is the floating gate transistor described in U.S. Patent 3,660,819, in which avalanche-injection is used to transfer charge to the electrically isolated gate of a field effect transistor. As disclosed in the patent, this semiconductor device structure provides the basis for an electrically alterable read-only-memory. Although this approach has proved useful, integrated circuit arrays of such semiconductor devices are inherently limited because of the spacing requirements associated with avalanche-injection.

Furthermore, during programming of the above device, avalanche-injection from the drain-substrate breakdown is used. The minimum channel length for a driver memory device of the above type is approximately  $0.45\text{ }\mu\text{m}$  for a  $-7.5$  volt drain voltage. For smaller channel lengths, a gate oxide breakdown will occur first. If the charging mechanism was other than avalanche-injection, the minimum channel length could be about  $0.25\text{ }\mu\text{m}$  for  $-2.0$  volt drain voltage, or even smaller for lower drain voltages. Also, during programming, the X and Y decoder devices in a memory, as above, operate at the programming voltages, e.g.  $-7.5$  volts. At this voltage, the minimum channel length is determined, as above, by drain-substrate breakdown.

To store a maximum charge of  $4 \times 10^{12}$  electrons/ $\text{cm}^2$  during avalanche-injection a gate charging current of about  $10^{-7}$  amp/ $\text{cm}^2$  is necessary for about 100 to 5000  $\mu$  seconds.

In extremely dense arrays of transistors or other semiconductor device structures, the use of avalanche-injection to create floating gates is not possible because the high voltages required for avalanche-injection cause voltage breakdown between adjacent device regions.

Additionally, with prior art devices as set forth above, only p-channel devices can be programmed without extensive modifications and/or extremely slow programming times.

The avalanche-injection technique stores a limited charge on the floating gate, because the charge injected to the gate alters the surface doping. Eventually, the drain-substrate breakdown is inhibited and the injection stops.

Another developing technology which relates to high density integrated circuit structures is electron beam technology. The advent of

computer controlled systems for rapidly positioning electron beams which have extremely small dimensions has made it possible to fabricate very small semiconductor devices. Dimensionally, electron beam fabrication systems can resolve lines and spaces as small as one-half micron. These computer controlled electron beam systems are also adapted for automatic registration so that the system can automatically locate and register on a particular location on a semiconductor wafer. A registration capability of this type makes it possible to preselect any particular region on any particular integrated circuit "chip" on a given semiconductor wafer. Additional details on computer controlled electron beam fabrication systems can be obtained by referring to the Technical Digest of the 1976 International Electron Devices Meeting, Session 18: "Device Technology-Electron Beam Technology and Applications," pps. 431-449.

Electron beams have also been proposed in various schemes for information storage including electrostatic storage on insulators, thermoplastic recording and electron beam exposure of photographic emulsions. One such scheme calls for applying a positive bias voltage to the metal gate of an insulated gate field effect transistor (IGFET) and then bombarding the gate with an electron beam. As a result of the bombardment, a positive charge accumulates in the gate oxide of the IGFET near the semiconductor oxide interface. The charge thus stored controls the conductive state of the IGFET and thereby provides the basis for an IGFET memory circuit. A complete discussion of this type IGFET memory is provided in the Proceedings of the IEEE, Volume 56, No. 2, February 1968, *An Electron Beam Activated Switch and Associated Memory*, page 158, McDonald and Eberhart. A particular constraint of this approach is that the electron beam voltage must be large enough to ensure complete penetration of the metal gate electrode of the IGFET and the associated oxide layer and the bombardment charge density must be sufficient to charge the oxide to saturation.

According to one aspect of the present invention there is provided a semiconductor memory device capable of being selectively programmed by an electron beam which comprises a substrate containing the device, a conductive region capable of storing charge from an electron beam overlying and electrically isolated from the substrate, an insulator layer overlying said conductive region and adapted to allow penetration by said electron beam and an electron beam registration element pre-aligned with said conductive region, for positioning said electron beam.

According to a further aspect of the present invention there is provided a method for manufacturing a semiconductor device comprising the steps of:

- a) providing a substrate containing said device;
- b) providing a conductive region which is

electrically isolated from said semiconductor device;

c) providing an electron beam registration element pre-aligned with said conductive region;

5 d) using said registration element to locate said conductive region; and

e) charging said conductive region with an electron beam to alter the operation of said semiconductor device.

10 According to yet a further aspect of the present invention we provide a storage device comprising:

a) a semiconductor body of a first conductivity type;

15 b) a pair of spaced apart regions of opposite conductivity type to said first conductivity type forming a pair of PN junctions in said body;

c) a floating gate disposed spatially between said pair of spaced apart regions;

20 d) an insulated layer between said body and said floating gate; and

e) insulative means covering said floating gate, said insulative means being free of any metallization employed primarily for charging said floating gate and said insulating means being of

25 prescribed thickness in the immediate region of said floating gate wherein an electron beam can cause electrons to pass through said region of prescribed thickness onto said floating gate whereby said floating gate may be electrically

30 charged.

According to yet a further aspect of the present invention we provide an insulated gate field effect transistor capable of being selectively

35 programmed by an electron beam for use in a memory array, said transistor comprising an electrically isolated gate electrode overlying a gate insulator layer and disposed spatially between a source region and a spaced apart drain region; an insulator layer overlying said gate

40 electrode and being of a thickness to allow penetration of electrons from an electron beam to said gate electrode; a region underlying said gate electrode, positioned between said source and

45 drain regions and having a conductive state responsive to electrons stored on said gate electrode from said electron beam and means for accurately positioning said electron beam with respect to said gate electrode.

According to another aspect of the invention

50 there is provided an electron beam programmable storage array comprising a plurality of memory elements on a substrate, each memory element including a conductive electrode capable of being programmed by storing charge

55 from an electron beam and a conductive registration element on said substrate formed simultaneously with and of the same material as said conductive electrode and located in relation to said memory elements for accurately

60 positioning said electron beam with respect to selected ones of said plurality of memory elements.

The invention will be more fully understood from the following description given by way of

65 example only in relation to the figures of the

accompanying drawing in which:—

Figure 1A through Figure 1E show cross-sectional views illustrating fabrication steps for producing a particular embodiment suitable for practicing the invention.

70 Figure 2 shows a top view of another particular embodiment suitable for practicing the invention;

Figure 3 shows a cross-sectional view of the particular embodiment of Figure 2;

75 Figure 4 shows a simplified block diagram of a computer controlled electron beam fabrication system as required for practicing the present invention;

80 Figure 5 shows a detailed view of an electron beam registration element as it would be located on a representative chip of the plurality of chips forming a semiconductor wafer.

Practice of the present invention requires a semiconductor device embodiment in which an electrically isolated conductor is adapted for charging by an electron beam. Figures 1A through 1E show cross-sectional views illustrating the fabrication steps by which such an embodiment can be made. Figure 1A shows the first step in the fabrication of a device structure 10 in which an N-type substrate of epi layer 12 is provided with an overlying layer 14 of silicon dioxide, which is typically about 5000 angstroms thick. (It should be noted that this description relates to P-channel

95 devices. The instant invention may also be practiced with N-channel devices with a P-substrate). In Figure 1B, conventional semiconductor processing techniques are used to define an active device region 16 and then to grow gate oxide layer 18, which is typically about 1000 angstroms thick. Figure 1C shows device structure 10 after the formation of a polysilicon gate 20, which is formed over a gate oxide region 22 by depositing a layer of polysilicon

105 approximately 5000 angstroms thick over the upper surface of gate oxide layer 18 and then etching to define source and drain regions 24 and 26. Figure 1D shows the next step in the process in which conventional diffusion and reoxidation

110 steps are used to form P+ diffused regions 28 and 30 by diffusing through the previously described openings 24 and 26. A thermal oxide layer 32, approximately 1000 angstroms thick, is formed coincident with the formation of diffused regions

115 28 and 30. Figure 1E shows the final form of semiconductor device structure 10. To attain this final structure, metal regions 34 and 36 are formed to contact diffused regions 28 and 30 through contact openings which are formed in

120 oxide layer 32 at locations 38 and 40 using conventional photomask and etching techniques. Typical procedures for forming metal regions 34 and 36 are to deposit 10,000 to 15,000 angstroms of aluminium over the upper surface of

125 the semiconductor device structure and to delineate the metal regions using conventional photomask and etching techniques. After metallization, a passivation layer 42 is formed over the upper surface of semiconductor device

130 structure 10. This layer is conventional except

that the final passivation etch process step (normally used to delineate the connection points or "pads" at the periphery of the semiconductor chip) is additionally used to create an opening or window 44 which exposes the upper surface of oxide layer 32 at a location where that oxide layer overlies conductive region 20. The formation of window 44 adapts semiconductor device structure 10 to allow an electric charge to be applied to conductive region 20 using an electron beam.

Semiconductor device structure 10, as shown in Figure 1E, illustrates one particular embodiment which is adapted to allow altered semiconductor device operation as a result of the application of an electron beam. In this case, metallic region 34 forms an electrical connection to diffused region 38 which functions as the source of a field effect transistor. In a similar fashion, metallic region 36 forms an electrical connection to diffused region 40 which forms the drain of the field effect transistor. Conductive region 20, which in this case is polysilicon, forms an electrically isolated or "floating" gate for the field effect transistor. As is well known for floating gate devices of this type, an electric charge stored on the gate will control the conductive or nonconductive state of the device. In conventional devices, this electric charge is stored on the floating gate by avalanche-injection. According to the present invention, semiconductor device 10, as shown in Figure 1E, differs in that it is adapted to allow the storage of electric charge applied by an electron beam. This difference provides several significant advantages. First, the use of an electron beam means that the location or spacing of the various diffused regions forming semiconductor device 10 are not constrained by the requirements of avalanche-injection. As a result, integrated circuits which are of much higher density and which are less expensive to manufacture can be achieved using the electron beam programmable device structure of the present invention. Another significant advantage of the device structure of the present invention is that it can be used to obtain field effect devices which are of either the enhancement mode type or the depletion mode type. This also allows the fabrication of devices using either P-channel or N-channel materials. These useful characteristics are obtained because the semiconductor device structure of the present invention can be adapted such that the electron beam procedure used to store electric charge on the isolated conductor (the floating gate 20 shown in Figure 1E) results in either positive or negative charging currents. The polarity of the charging current is determined by the thickness of the overlying oxide layer (such as oxide layer 32 shown in Figure 1D) relative to the energy of the primary electron beam used to apply charge to the isolated conductor. Additional information regarding the energy interrelationships of negative or positive charging currents can be obtained by referring to the textbook, "Scanning Electron Microscopy", by P.

R. Thornton, copyright 1968, Chapman and Hall, Ltd., London, pages 111 through 115.

The elementary semiconductor device structure 10 shown in Figure 1E provides a building block which can be employed in a wide variety of devices. It is not, however, the only embodiment suitable for practicing the invention as shown by the different embodiments of Figures 2 and 3. Figure 2 shows a schematic top view of a portion of an electron beam programmable storage array 100. Figure 3 shows a representative cross-sectional view of storage array 100 corresponding to section line X—X' shown in Figure 2. Storage array 100 comprises a substrate 102 in which there are disposed a plurality of diffused regions such as representative diffused region 104 arranged as a parallel grid. The upper surface of the substrate 102 is covered with an insulating layer upon which a plurality of conductive regions are formed. Figure 2 and Figure 3 show a representative conductive region 106. The plurality of conductive regions such as region 106 are arranged as a parallel grid which is generally orthogonal to the parallel grid of diffused regions represented by region 104. Storage array 100 also includes a plurality of conductive elements such as representative element 108. Each of these conductive elements is positioned adjacent to the intersection of diffused region and an overlying conductive region but each of these conductive elements is electrically isolated from each of them as shown by the relative position of representative conductive element 108 in Figures 2 and 3. An aperture or window is formed in insulative layer 110 in the vicinity of each of the conductive elements. Thus, Figure 2 and Figure 3 show a representative aperture 112 formed in conjunction with conductive element 108. The plurality of apertures such as representative aperture 112 adapt storage array 100 for electron beam programming since they provide locations where the thickness of overlying insulative layer 110 is reduced enough to allow electron beam penetration and subsequent storage of electric charge on the conductive elements of the array such as representative element 108. Storage array 100 is a capacitive storage array in which there is an equivalent capacitance formed at each intersection of the orthogonal grids formed by the diffused and the conductive regions. The value of this equivalent capacitance is a function of the electric charge present on the conductive elements present at each intersection. Thus, the use of an electron beam to program the stored charge and to therefore determine the capacitance of each element of the array results in a programmable storage array which has very simple structure. This simple structure allows the fabrication of a very high density array. When electron beam fabrication methods such as those previously referenced are used, it is possible to fabricate a storage array comprising an orthogonal grid of one micron wide diffused regions and one micron wide conductive regions

each spaced one micron apart. With such a storage array, one million bits of digital information can be stored in a square storage array region which is 55 mils on each side.

5 Figure 4 shows a simplified block and pictorial diagram of a computer controlled electron beam system 200 of the type which would be used to program electron beam programmable semiconductor devices according to the present invention. System 200 comprises a computer control circuit 202 which couples via control link 204 to deflection control circuit 206. Deflection control circuit 206 couples to a magnetic yoke 208 and electrostatic deflection plates 210 which function in combination to focus and position electron beam 212. Electron beam 212 is accelerated by a voltage source (not shown) to impinge on the surface of a semiconductor wafer 214 which is affixed to a movable wafer mount 216. The impinging of electron beam 212 on the surface of wafer 214 produces backscatter of secondary electrons which are detected by detectors 218 which are coupled to deflection detection circuit 220. Deflection detection circuit 220 functions to produce signals which indicate the position of the electron beams 212. These signals are coupled to computer controller 202 via control link 222. Computer control circuit 202 interprets the received position signals and, in accordance with the algorithm of its stored program, produces control signals on control link 224 which is coupled to chip position control circuit 226. Chip position control circuit 226 produces an X direction control output 228 and a Y direction control output 230 which are coupled as inputs to movable wafer mount 216 and thereby determine the magnitude and direction of its movement.

The operation of the electron beam positioning system shown in Figure 4 requires that the electron beam be accurately positioned within the periphery of a single one of the plurality of chips which form a semiconductor wafer. The detailed view of Figure 5 shows how this can be accomplished. In Figure 5, a particular semiconductor chip 232, which is physically similar to adjacent chips 234, 236, 238, is required to be correctly positioned with respect to electron beam 212. This is accomplished through the use of a registration element 240. The particular shape chosen for registration element 240 guarantees that a unique pattern of back scattered secondary electrons will be produced when registration element 240 is traversed by electron beam 212 in the X direction and in the Y direction. Precise positioning is further determined by insuring that registration element 240 is prealigned with respect to the electron beam programmable elements of the semiconductor devices forming the storage array (designated schematically as array 242 in Figure 5). This prealignment is accomplished by fabricating registration element 240 during the same process step as the electron beam programmable elements of the storage array are

fabricated. Thus, for the particular case of an array of floating gate field effect devices, registration element 240 would be fabricated by depositing and then etching polysilicon at the same time (and using the same mask) as when the polysilicon "floating gates" were formed.

#### Claims

1. A semiconductor memory device capable of being selectively programmed by an electron beam which comprises a substrate containing the device, a conductive region capable of storing charge from an electron beam overlying and electrically isolated from the substrate, an insulator layer overlying said conductive region and adapted to allow penetration by said electron beam and an electron beam registration element pre-aligned with said conductive region, for positioning said electron beam.
2. A method for manufacturing a semiconductor device comprising the steps of:
  - a) providing a substrate containing said device;
  - b) providing a conductive region which is electrically isolated from said semiconductor device;
  - c) providing an electron beam registration element pre-aligned with said conductive region;
  - d) using said registration element to locate said conductive region; and
  - e) charging said conductive region with an electron beam to alter the operation of said semiconductor device.
3. A storage device comprising:
  - a) a semiconductor body of a first conductivity type;
  - b) a pair of spaced apart regions of opposite conductivity type to said first conductivity type forming a pair of PN junctions in said body;
  - c) a floating gate disposed spatially between said pair of spaced apart regions;
  - d) an insulated layer between said body and said floating gate; and
  - e) insulating means covering said floating gate, said insulating means being free of any metallization employed primarily for charging said floating gate and said insulative means being of prescribed thickness in the immediate region of said floating gate wherein an electron beam can cause electrons to pass through said region of prescribed thickness onto said floating gate whereby said floating gate may be electrically charged.
4. An insulated gate field effect transistor capable of being selectively programmed by an electron beam for use in a memory array, said transistor comprising an electrically isolated gate electrode overlying a gate insulator layer and disposed spatially between a source region and a spaced apart drain region; an insulator layer overlying said gate electrode and being of a thickness to allow penetration of electrons from an electron beam to said gate electrode; a region underlying said gate electrode, positioned between said source and drain regions and having a conductive state responsive to electrons stored



each spaced one micron apart. With such a storage array, one million bits of digital information can be stored in a square storage array region which is 55 mils on each side.

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The operation of the electron beam positioning system shown in Figure 4 requires that the electron beam be accurately positioned within the periphery of a single one of the plurality of chips which form a semiconductor wafer. The detailed view of Figure 5 shows how this can be accomplished. In Figure 5, a particular semiconductor chip 232, which is physically similar to adjacent chips 234, 236, 238, is required to be correctly positioned with respect to electron beam 212. This is accomplished through the use of a registration element 240. The particular shape chosen for registration element 240 guarantees that a unique pattern of back scattered secondary electrons will be produced when registration element 240 is traversed by electron beam 212 in the X direction and in the Y direction. Precise positioning is further determined by insuring that registration element 240 is prealigned with respect to the electron beam programmable elements of the semiconductor devices forming the storage array (designated schematically as array 242 in Figure 5). This prealignment is accomplished by fabricating registration element 240 during the same process step as the electron beam programmable elements of the storage array are

fabricated. Thus, for the particular case of an array of floating gate field effect devices, registration element 240 would be fabricated by depositing and then etching polysilicon at the same time (and using the same mask) as when the polysilicon "floating gates" were formed.

#### Claims

1. A semiconductor memory device capable of being selectively programmed by an electron beam which comprises a substrate containing the device, a conductive region capable of storing charge from an electron beam overlying and electrically isolated from the substrate, an insulator layer overlying said conductive region and adapted to allow penetration by said electron beam and an electron beam registration element pre-aligned with said conductive region, for positioning said electron beam.

2. A method for manufacturing a semiconductor device comprising the steps of:  
a) providing a substrate containing said device;  
b) providing a conductive region which is electrically isolated from said semiconductor device;

c) providing an electron beam registration element pre-aligned with said conductive region;  
d) using said registration element to locate said conductive region; and

e) charging said conductive region with an electron beam to alter the operation of said semiconductor device.

3. A storage device comprising:

a) a semiconductor body of a first conductivity type;

b) a pair of spaced apart regions of opposite conductivity type to said first conductivity type forming a pair of PN junctions in said body;

c) a floating gate disposed spatially between said pair of spaced apart regions;

d) an insulated layer between said body and said floating gate; and

e) insulating means covering said floating gate, said insulating means being free of any metallization employed primarily for charging said floating gate and said insulative means being of prescribed thickness in the immediate region of said floating gate wherein an electron beam can cause electrons to pass through said region of prescribed thickness onto said floating gate whereby said floating gate may be electrically charged.

4. An insulated gate field effect transistor capable of being selectively programmed by an electron beam for use in a memory array, said transistor comprising an electrically isolated gate electrode overlying a gate insulator layer and disposed spatially between a source region and a spaced apart drain region; an insulator layer overlying said gate electrode and being of a thickness to allow penetration of electrons from an electron beam to said gate electrode; a region underlying said gate electrode, positioned between said source and drain regions and having a conductive state responsive to electrons stored



on said gate electrode from said electron beam and means for accurately positioning said electron beam with respect to said gate electrode.

- 5 An electron beam programmable storage array comprising a plurality of memory elements on a substrate, each memory element including a conductive electrode capable of being programmed by storing charge from an electron beam and a conductive registration element on
- 10 said substrate formed simultaneously with and of the same material as said conductive electrode and located in relation to said memory elements

for accurately positioning said electron beam with respect to selected ones of said plurality of memory elements.

- 15 6. A semiconductor device constructed and arranged substantially as herein described and as shown in Figures of the accompanying drawing.
7. A method for manufacturing a
- 20 semiconductor device as herein described and as shown in the Figures of the accompanying drawing.
8. A semiconductor device whenever made by the method of Claim 2.