ABSTRACT

A METHOD OF CONTROLLED LOW-K VIA ETCH FOR CU INTERCONNECTIONS

An interconnect stack and a method of manufacturing the same wherein the interconnect has vertical sidewall vias. The interconnect stack includes a substrate, a metal interconnect formed in the substrate, an etch stop formed on the substrate and the metal interconnect, and an interlayer dielectric (ILD) layer having at least one via formed therein extending through a transition layer formed on the etch stop layer. The via is formed by etching the ILD to a first depth and ashing the interconnect stack to modify a portion of the ILD between the portion of the via formed by etching and the transition layer. Ashing converts this portion of the ILD to an oxide material. The method includes wet etching the interconnect to remove the oxide material and a portion of the transition layer to form a via extending through the ILD to the etch stop layer.

Fig 5