

THIS SHEET HAS BEEN
REPLACED

MEMORY CONTROLLER FOR DIRECT OR INTERLEAVE
MEMORY ACCESSING

ABSTRACT

A data processing system includes a processor for accessing a memory in either a direct mode or an indirect mode. The memory includes at least two memory banks and two decoders for decoding bank addresses. The decoders produce bank select signals. In direct mode, the decoder outputs are generated according to which bank is addressed. In interleaved mode, the two decoder outputs are ANDed to select both banks covering the address range of the selected banks.

This Sheet Has Been Replaced

