(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 September 2009 (03.09.2009)

PCT

(10) International Publication Number
WO 2009/106330 A1

(51) International Patent Classification:
H01L 31/18 (2006.01) *H01L 27/146* (2006.01)

(21) International Application Number:
PCT/EP2009/001382

(22) International Filing Date:
26 February 2009 (26.02.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
08290176.0 26 February 2008 (26.02.2008) EP
09290097.6 11 February 2009 (11.02.2009) EP

(71) Applicant *(for all designated States except US)*: **S.O.I. TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Chemin des Franques, Parc Technologique des Fontaines, F-38190 Bernin (FR).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **DROUIN, Alexis** [FR/FR]; Residence Ie Vieux Logis, 99 bis Grande Rue, F-38700 La Tranche (FR). **ASPAR, Berhard** [FR/FR]; Lot. L'Abri Dauphinois, Chemin Ribotiere, F-38330 Saint lsmier (FR). **DESRUMEAUX, Christophe** [FR/FR]; 605 rue du Chateau Dauphin, F-38530 La Buissiere (FR). **LEDOUX, Olivier** [FR/FR]; 11 rue Massena, F-38000 Grenoble (FR). **FIGUET, Christophe** [FR/FR]; 438 rue Hector Berlioz, F-38920 Crolles (FR).

(74) Agent: **NEUBECK, Wolfgang**; Grünecker, Kinkeldey, Stockmair & Schwanhausser, LeopoldstraBe 4, 80802 Miinchen (DE).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

[Continued on next page]

(54) Title: METHOD FOR FABRICATING A SEMICONDUCTOR SUBSTRATE

(57) Abstract: The invention relates to a method for fabricating a semiconductor substrate comprising the steps of: providing a silicon on insulator type substrate comprising a base, an insulating layer and a first semiconductor layer, doping the first semiconductor layer to thereby obtain a modified first semiconductor layer, and providing a second semiconductor layer with a different dopant concentration than the modified first semiconductor layer over, in particular on, the modified first semiconductor layer. With this method, an improved dopant concentration profile can be achieved through the various layers which makes the substrates in particular suitable for optoelectronic applications.

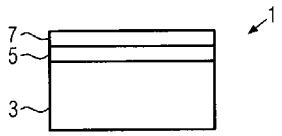


FIG. 1a

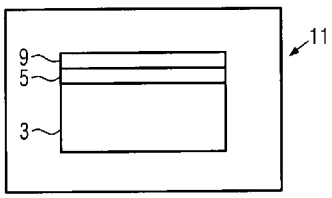


FIG. 1b

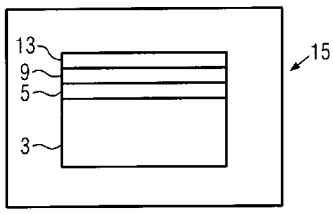


FIG. 1c

WO 2009/106330 A1

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*