(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 March 2011 (03.03.2011)

PCT

(10) International Publication Number
WO 2011/024619 A1

(51) International Patent Classification:
H01L 21/02 (2006.01) *H01L 27/12* (2006.01)
H01L 21/20 (2006.01) *H01L 29/786* (2006.01)
H01L 21/336 (2006.01)

(21) International Application Number:
PCT/JP2010/063142

(22) International Filing Date:
28 July 2010 (28.07.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2009-194182 25 August 2009 (25.08.2009) JP

(71) Applicant *(for all designated States except US)*: **SEMICONDUCTOR ENERGY LABORATORY CO., LTD.** [JP/JP]; 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **HANAOKA, Kazuya** [JP/JP]; c/o SEMICONDUCTOR ENERGY LABORATORY CO., LTD., 398, Hase, Atsugi-shi, Kanagawa, 2430036 (JP). **IMAI, Keitaro**.

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: METHOD FOR REPROCESSING SEMICONDUCTOR SUBSTRATE, METHOD FOR MANUFACTURING REPROCESSED SEMICONDUCTOR SUBSTRATE, AND METHOD FOR MANUFACTURING SOI SUBSTRATE

FIG. 1A

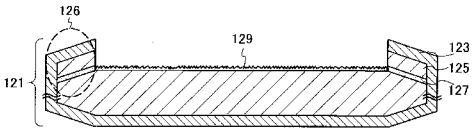


FIG. 1B

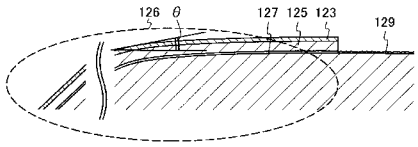


FIG. 1C

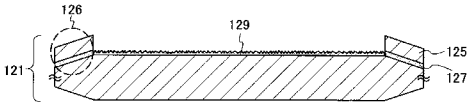
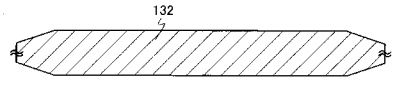


FIG. 1D



(57) **Abstract**: An object is to provide a method suitable for reprocessing a semiconductor substrate which is reused to manufacture an SOI substrate. A semiconductor substrate is reprocessed in the following manner: etching treatment is performed on a semiconductor substrate in which a projection including a damaged semiconductor region and an insulating layer exists in a peripheral portion, whereby the insulating layer is removed; and etching treatment is performed on the semiconductor substrate with the use of a mixed solution including a substance that oxidizes a semiconductor material included in the semiconductor substrate, a substance that dissolves the oxidized semiconductor material, and a substance that controls oxidation speed of the semiconductor material and dissolution speed of the oxidized semiconductor material, whereby the damaged semiconductor region is selectively removed with a non-damaged semiconductor region left.

WO 2011/024619 A1