What is Claimed is:

1. A semiconductor memory device, comprising:

a lower dielectric layer;

a bit line that extends in a first direction on the lower dielectric layer;

a first word line and a second word line that extend in a second direction and cross the bit line;

an active pattern on the bit line between the first word line and the second word line, the active pattern comprising a first vertical part and a second vertical part that are opposite to each other, and a horizontal part that extends between the first vertical part and the second vertical part;

a first data storage pattern between the first word line and the first vertical part of the active pattern;

a second data storage pattern between the second word line and the second vertical part of the active pattern; and

a source line connected to the active pattern, the source line extending the first direction and crossing the first word line and the second word line,

wherein the first direction and the second direction are parallel to a top surface of the lower dielectric layer.

2. The semiconductor memory device of claim 1, wherein the active pattern comprises an oxide semiconductor.

3. The semiconductor memory device of claim 1 or claim 2, wherein the first data storage pattern and the second data storage pattern comprise a ferroelectric material.

4. The semiconductor memory device of any one of claims 1 to 3, wherein the first data storage pattern and the second data storage pattern extend in the second direction on the bit line.

5. The semiconductor memory device of any one of claims 1 to 4, wherein, when viewed in vertical section, the first word line and the second word line are between the bit line and the source line.

6. The semiconductor memory device of any one of claims 1 to 5, wherein the source line is electrically connected to the first vertical part or the second vertical part of the active pattern.

7. The semiconductor memory device of any one of claims 1 to 6, wherein top surfaces of the first vertical part and a top surface of the second vertical part are substantially coplanar with top surfaces of the first data storage pattern and the second data storage pattern.

8. The semiconductor memory device of any one of claims 1 to 6, wherein top surfaces of the first data storage pattern and the second data storage pattern are substantially coplanar with top surfaces of the first word line and the second word line.

9. The semiconductor memory device of any one of claims 1 to 8, further comprising lower dielectric patterns that extend in the second direction between a top surface of the bit line and bottom surfaces of the first word line and the second word line.

10. The semiconductor memory device of any one of claims 1 to 9, further comprising:

a first contact pad coupled to the first vertical part of the active pattern;

a second contact pad coupled to the second vertical part of the active pattern;

a first contact pattern coupled to the first contact pad; and

a second contact pattern coupled to the second contact pad,

wherein, when viewed in plan, the first contact pattern and the second contact pattern are spaced apart from each other across the bit line.

11. The semiconductor memory device of claim 10, wherein the source line comprises:

a first source line that extends in the first direction and is connected to the first contact pattern; and

a second source line that extends in the first direction and is connected to the second contact pattern.

12. The semiconductor memory device of claim 1, wherein the active pattern further comprises:

a first upper horizontal part on the first word line and connected to the first vertical part; and

a second upper horizontal part on the second word line and connected to the second vertical part.

13. The semiconductor memory device of claim 12, further comprising:

a first upper dielectric pattern between the first upper horizontal part of the active pattern and a top surface of the first word line; and

a second upper dielectric pattern between the second upper horizontal part of the active pattern and a top surface of the second word line.

14. A semiconductor memory device, comprising:

bit lines that extend in a first direction and are spaced apart from each other in a second direction that crosses the first direction;

first word lines and second word lines that extend in the second direction, cross the bit lines and are alternately arranged along the first direction;

active patterns on each of the bit lines and each of regions between the first word lines and the second word lines, each of the active patterns comprising a first vertical part and a second vertical part that are opposite to each other and a horizontal part that extends between the first vertical part and the second vertical part;

first ferroelectric patterns between the first word lines and the first vertical part of the active patterns;

second ferroelectric patterns between the second word lines and the second vertical part of the active patterns;

first source lines and second source lines that extend in the first direction and cross the first word lines and the second word lines; and

shield lines disposed between the bit lines, respectively and extending in the first direction.

15. The semiconductor memory device of claim 14, further comprising:

first contact pads respectively coupled to the first vertical part of the active patterns;

second contact pads respectively coupled to the second vertical part of the active patterns;

first contact patterns respectively coupled to the first contact pads; and

second contact patterns respectively coupled to the second contact pads,

wherein, when viewed in plan, the first contact patterns and the second contact patterns are spaced apart from each other across the bit lines.

16. The semiconductor memory device of claim 15, wherein each of the first source lines is connected to the first contact patterns arranged along the first direction, and

wherein each of the second source lines is connected to the second contact patterns arranged along the first direction.

17. The semiconductor memory device of any one of claims 14 to 16, wherein the first ferroelectric patterns and the second ferroelectric patterns extend in the second direction on the bit lines.

18. The semiconductor memory device of any one of claims 14 to 17, wherein the first ferroelectric patterns are in direct contact with the first vertical part of the active patterns, and

wherein the second ferroelectric patterns are in direct contact with the second vertical part of the active patterns.

19. The semiconductor memory device of any one of claims 14 to 18, further comprising a peripheral circuit structure that comprises peripheral circuits on a semiconductor substrate and a lower dielectric layer that covers the peripheral circuits,

wherein the bit lines are on the lower dielectric layer.

20. A semiconductor memory device, comprising a plurality of cell array layers that are vertically stacked on a lower dielectric layer, wherein each of the plurality of cell array layers comprises:

a bit line that extends in a first direction;

a first word line and a second word line that extend in a second direction and cross the bit line;

an active pattern on the bit line between the first word line and the second word line, the active pattern comprising a first vertical part and a second vertical part that are opposite to each other, and a horizontal part that extends between the first vertical part and the second vertical part;

a first data storage pattern between the first word line and the first vertical part of the active pattern;

a second data storage pattern between the second word line and the second vertical part of the active pattern; and

a source line that extends in the first direction and crosses the first word line and the second word line.