CLAIMS

What is claimed is :

1. A microelectronic device, comprising:

an assembly comprising:

a memory array region comprising:

a stack structure comprising vertically alternating conductive structures and insulating structures; and

strings of memory cells respectively vertically extending through the stack structure; and

digit lines overlying the stack structure and coupled to the strings of memory cells;

a control logic region underlying the stack structure and comprising control logic devices configured to effectuate a portion of control operations for the strings of memory cells;

an additional control logic region overlying the digit lines and comprising additional control logic devices configured to effectuate an additional portion of the control operations for the vertically extending strings of memory cells;

conductive pad structures underlying the stack structure and electrically connected to the control logic devices;

additional conductive pad structures overlying the stack structure and electrically connected to the additional control logic devices; and

at least one conductive contact structure vertically extending completely through the stack structure and electrically connected to at least one of the conductive pad structures and at least one of the additional conductive pad structures; and

a microelectronic device structure attached to the assembly and including:

an additional memory array region underlying the control logic region and comprising:

an additional stack structure comprising vertically alternating additional conductive structures and additional insulating structures; and

additional strings of memory cells respectively vertically extending through the additional stack structure;

additional digit lines overlying the additional stack structure and coupled to the additional strings of memory cells; and

a further control logic region underlying the additional memory array region and comprising further control logic devices configured to effectuate a portion of control operations for the additional strings of memory cells of the additional memory array region.

2. The microelectronic device of claim 1, wherein the additional control logic devices of the additional control logic region are configured to operate at applied voltages less than or equal to 1.4 V.

3. The microelectronic device of claim 1, wherein the additional control logic devices of the additional control logic region are configured to operate at applied voltages within a range of from 0.7V to 1.3 V.

4. The microelectronic device of claim 1, wherein the control logic devices and the additional control logic devices each individually comprise CMOS circuitry.

5. The microelectronic device of claim 1, further comprising:

conductive line structures vertically between the stack structure and the additional conductive pad structures;

conductive routing structures vertically between the conductive line structures and the additional conductive pad structures; and

interconnect structures vertically between the conductive routing structures and the additional conductive pad structures.

6. The microelectronic device of claim 5, wherein:

the conductive routing structures comprise aluminum; and

the interconnect structures comprise copper.

7. A microelectronic device, comprising:

an assembly comprising:

a memory array region comprising:

a stack structure comprising vertically alternating conductive structures and insulating structures; and

vertically extending strings of memory cells within the stack structure;

digit lines overlying the stack structure and coupled to the strings of memory cells;

a control logic region underlying the stack structure and comprising control logic devices configured to effectuate a portion of control operations for the vertically extending strings of memory cells;

an additional control logic region overlying the digit lines and comprising additional control logic devices configured to effectuate an additional portion of the control operations for the vertically extending strings of memory cells; and

a microelectronic device structure attached to the assembly and including:

an additional memory array region underlying the control logic region of the assembly and comprising:

an additional stack structure comprising vertically alternating additional conductive structures and additional insulating structures; and

additional vertically extending strings of memory cells within the additional stack structure; and

additional digit lines overlying the additional stack structure and coupled to the additional vertically extending strings of memory cells; and

a further control logic region underlying the additional memory array region and comprising further control logic devices configured to effectuate a portion of control operations for the additional vertically extending strings of memory cells of the additional memory array region.

8. A method of forming a microelectronic device, comprising:

forming a first microelectronic device structure comprising:

a control logic region comprising control logic devices; and

a memory array region over the control logic region and comprising:

conductive pad structures electrically connected to the control logic devices;

a stack structure over the conductive pad structures and comprising vertically alternating conductive structures and insulating structures;

additional conductive pad structures overlying the stack structure;

strings of memory cells respectively vertically extending through the stack structure;

digit lines overlying the stack structure and coupled to the strings of memory cells; and

at least one conductive contact structure vertically extending completely through the stack structure and electrically connected to at least one of the conductive pad structures and at least one of the additional conductive pad structures;

forming a second microelectronic device structure comprising an additional control logic region comprising additional control logic devices;

attaching the first microelectronic device structure to the second microelectronic device structure to form an assembly including the stack structure vertically intervening between the control logic region and the additional control logic region, and including the additional conductive pad structures are electrically connected to the additional control logic devices; and

forming a third microelectronic device structure comprising:

a further control logic region comprising further control logic devices; and

an additional memory array region over the further control logic region, the additional memory array region comprising:

an additional stack structure comprising vertically alternating additional conductive structures and additional insulating structures;

additional strings of memory cells respectively vertically extending through the additional stack structure; and

additional digit lines overlying the additional stack structure and coupled to the additional strings of memory cells; and

attaching the assembly to the third microelectronic device structure to form a construction including the control logic region overlying the further control logic region, and the additional control logic region overlying the control logic region.

9. The method of claim 8, further comprising selecting the additional control logic devices to comprise CMOS circuitry configured to operate at applied voltages within a range of from 0.7 V to 1.4 V.

10. The method of claim 9, further comprising selecting the control logic devices to comprise additional CMOS circuitry configured to operate at other applied voltages greater than the applied voltages effective to operate of the CMOS circuitry of the additional control logic devices.

11. A method of forming a microelectronic device, comprising:

forming a first microelectronic device structure comprising:

a control logic region comprising control logic devices; and

a memory array region over the control logic region and comprising:

a stack structure comprising vertically alternating conductive structures and insulating structures; and

vertically extending strings of memory cells within the stack structure; and

digit lines overlying the stack structure and coupled to the vertically extending strings of memory cells;

forming a second microelectronic device structure comprising an additional control logic region comprising additional control logic devices;

attaching the first microelectronic device structure to the second microelectronic device structure to form an assembly including the stack structure vertically intervening between the control logic region and the additional control logic region;

forming a third microelectronic device structure comprising:

a further control logic region comprising further control logic devices; and

an additional memory array region over the further control logic region and comprising:

an additional stack structure comprising vertically alternating additional conductive structures and additional insulating structures;

additional vertically extending strings of memory cells within the additional stack structure; and

additional digit lines overlying the additional stack structure and coupled to the additional vertically extending strings of memory cells; and

attaching assembly to the third microelectronic device structure to form a construction including the control logic region overlying the further control logic region, and the additional control logic region overlying the control logic region.