

MEMORY DEVICE AND METHOD OF OPERATING THE MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

5 **[0001]** The present application claims priority under 35 U.S.C. § 119(a) to Korean patent application number 10-2019-0100570 filed on August 16, 2019, in the Korean Intellectual Property Office, the entire disclosure of which is incorporated herein by reference.

BACKGROUND

10 1. Technical Field

[0002] Various embodiments of the present disclosure generally relate to an electronic device, and more particularly, to a memory device and a method of operating the memory device.

2. Related Art

15 **[0003]** A storage device is a device which stores data under the control of a host device, such as a computer or a smartphone. The storage device may include a memory device in which data is stored and a memory controller which controls the memory device. Such memory devices are classified into a volatile memory device and a nonvolatile memory device.

20 **[0004]** The volatile memory device is a memory device in which data is stored only when power is supplied and in which stored data is lost when the supply of power is interrupted. Examples of the volatile memory device include a Static Random Access Memory (SRAM) and a Dynamic Random Access Memory (DRAM).

[0005] The nonvolatile memory device is a memory device in which stored data is retained even when the supply of power is interrupted. Examples of the nonvolatile memory device include a Read Only Memory (ROM), a Programmable ROM (PROM), an Electrically Programmable ROM (EPROM),
5 an Electrically Erasable and Programmable ROM (EEPROM), and a flash memory.

SUMMARY

[0006] An embodiment of the present disclosure may provide for a memory device. The memory device may include a memory cell array, a
10 plurality of page buffer groups, and a program operation controller. The memory cell array may include a plurality of memory cells. The page buffer groups may be coupled to the plurality of memory cells through a plurality of bit line groups, and may be configured to perform bit line precharge operations on the plurality of bit line groups. The program
15 operation controller may be configured to control the plurality of page buffer groups to perform the bit line precharge operations initiated at different time points during a program operation on the plurality of memory cells, and to adjust an interval between initiation time points of the bit line precharge operations depending on a progress of the program
20 operation.

[0007] An embodiment of the present disclosure may provide for a method of operating a memory device, the memory device performing a program operation on a plurality of memory cells. The method may include determining an interval between initiation time points of bit line precharge

operations on a plurality of bit line groups coupled to the plurality of memory cells depending on a progress of the program operation, and performing the bit line precharge operations depending on the determined interval between the initiation time points.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a diagram illustrating a storage device according to an embodiment of the present disclosure.

[0009] FIG. 2 is a diagram illustrating the structure of a memory device of FIG. 1.

10 **[0010]** FIG. 3 is a diagram illustrating a memory cell array of FIG. 2.

[0011] FIG. 4 is a diagram illustrating a program operation according to an embodiment.

[0012] FIG. 5 is a diagram illustrating a progress sequence of a program operation according to an embodiment.

15 **[0013]** FIG. 6 is a diagram for explaining bit line loading.

[0014] FIG. 7 is a diagram for explaining a change in bit line loading depending on the progress of a program operation.

[0015] FIG. 8 is a diagram illustrating the configuration and operation of a memory device according to an embodiment.

20 **[0016]** FIG. 9 is a diagram illustrating a read and write circuit of FIG. 8.

[0017] FIG. 10 is a diagram illustrating a program voltage apply step of FIG. 4.

[0018] FIG. 11 is a diagram illustrating a bit line precharge operation according to an embodiment.

[0019] FIG. 12 is a diagram illustrating a bit line precharge operation according to an embodiment.

[0020] FIG. 13 is a diagram illustrating an operation of adjusting an interval between initiation time points of the bit line precharge operation of FIG. 12.

[0021] FIG. 14 is a flowchart illustrating a program operation according to an embodiment.

[0022] FIG. 15 is a flowchart illustrating the program operation of FIG. 14 according to an embodiment.

[0023] FIG. 16 is a flowchart illustrating the program operation of FIG. 14 according to an embodiment.

DETAILED DESCRIPTION

[0024] Specific structural or functional descriptions in the embodiments of the present disclosure introduced in this specification or application are only for description of the embodiments of the present disclosure. The descriptions should not be construed as being limited to the embodiments described in the specification or application.

[0025] Various embodiments of the present disclosure are directed to a memory device having improved bit line precharge performance and a method of operating the memory device.

[0026] FIG. 1 is a diagram illustrating a storage device according to an embodiment of the present disclosure.

[0027] Referring to FIG. 1, a storage device 50 may include a memory

device 100 and a memory controller 200 which controls the operation of the memory device. The storage device 50 may be a device which stores data under the control of a host, such as a mobile phone, a smartphone, an MP3 player, a laptop computer, a desktop computer, a game console, a television (TV), a tablet PC, or an in-vehicle infotainment system.

[0028] The storage device 50 may be manufactured as any one of various types of storage devices depending on a host interface that is a communication scheme with the host. The storage device 50 may be implemented as any one of various types of storage devices, for example, a solid state drive (SSD), a multimedia card such as an MMC, an embedded MMC (eMMC), a reduced size MMC (RS-MMC), or a micro-MMC, a secure digital card such as an SD, a mini-SD, or a micro-SD, a universal storage bus (USB) storage device, a universal flash storage (UFS) device, a personal computer memory card international association (PCMCIA) card-type storage device, a peripheral component interconnection (PCI)-card type storage device, a PCI express (PCI-E) card-type storage device, a compact flash (CF) card, a smart media card, and a memory stick.

[0029] The storage device 50 may be manufactured in any one of various types of package forms. For example, the storage device 50 may be manufactured in any one of various types of package forms, such as package on package (POP), system in package (SIP), system on chip (SOC), multi-chip package (MCP), chip on board (COB), wafer-level fabricated package (WFP), and wafer-level stack package (WSP).

[0030] The memory device 100 may store data. The memory device 100

is operated in response to the control of the memory controller 200. The memory device 100 may include a memory cell array including a plurality of memory cells which store data.

[0031] Each of the memory cells may be implemented as a single-level cell (SLC) capable of storing a single data bit, a multi-level cell (MLC) capable of storing two data bits, a triple-level cell (TLC) capable of storing three data bits, or a quad-level cell (QLC) capable of storing four data bits.

[0032] The memory cell array may include a plurality of memory blocks. Each memory block may include a plurality of memory cells. A single memory block may include a plurality of pages. In an embodiment, each page may be a unit by which data is stored in the memory device 100 or by which data stored in the memory device 100 is read.

[0033] A memory block may be a unit by which data is erased. In an embodiment, the memory device 100 may take many alternative forms, such as a double data rate synchronous dynamic random access memory (DDR SDRAM), a low power double data rate fourth generation (LPDDR4) SDRAM, a graphics double data rate (GDDR) SDRAM, a low power DDR (LPDDR) SDRAM, a Rambus dynamic random access memory (RDRAM), a NAND flash memory, a vertical NAND flash memory, a NOR flash memory device, a resistive RAM (RRAM), a phase-change memory (PRAM), a magnetoresistive RAM (MRAM), a ferroelectric RAM (FRAM), or a spin transfer torque RAM (STT-RAM). In the present specification, for convenience of description, a description will be made on the assumption that the memory device 100 is a NAND flash memory.

[0034] The memory device 100 may receive a command and an address from the memory controller 200, and may access the area of the memory cell array, selected by the address. That is, the memory device 100 may perform an operation indicated by the command on the area selected by the address. For example, the memory device 100 may perform a write operation (i.e., program operation), a read operation, and an erase operation. During a program operation, the memory device 100 may program data to the area selected by the address. During a read operation, the memory device 100 may read data from the area selected by the address. During an erase operation, the memory device 100 may erase data stored in the area selected by the address.

[0035] In an embodiment, the memory device 100 may include a read and write circuit 123 and a program operation controller 131.

[0036] The read and write circuit 123 may include a plurality of page buffer groups coupled to the memory cells of the memory cell array through bit lines. The bit lines may be divided into a plurality of bit line groups respectively corresponding to a plurality of page buffer groups. The plurality of page buffer groups may perform bit line precharge operations of precharging the plurality of bit line groups corresponding thereto, respectively, during a program operation performed on the memory cells.

[0037] The program operation controller 131 may control the plurality of page buffer groups so that the respective page buffer groups initiate bit line precharge operations at different time points. The program

operation controller 131 may adjust an interval (i.e., time gap) between the initiation time points of the bit line precharge operations performed by respective page buffer groups depending on the progress of the program operation.

5 **[0038]** The progress of the program operation may be determined to be a highest program state, among program states for which a program verify operation has passed. The highest program state for which the program verify operation has passed will be described later with reference to FIG. 5. Alternatively, the progress of the program operation may be determined
10 to be a program loop count indicating the number of program loops that have been performed, among one or more program loops that are performed during the program operation. The program loops will be described later with reference to FIG. 4.

[0039] The memory controller 200 controls the overall operation of the
15 storage device 50.

[0040] When power is applied to the storage device 50, the memory controller 200 may run firmware (FW). When the memory device 100 is a flash memory device, the memory controller 200 may run firmware such as a Flash Translation Layer (FTL) for controlling communication
20 between the host and the memory device 100.

[0041] In an embodiment, the memory controller 200 may receive data and a logical block address (LBA) from the host, and may translate the logical block address (LBA) into a physical block address (PBA) indicating the address of memory cells which are included in the memory device 100

and in which data is to be stored.

[0042] The memory controller 200 may control the memory device 100 so that a program operation, a read operation or an erase operation is performed in response to a request received from the host. During a
5 program operation, the memory controller 200 may provide a write command, a physical block address (PBA), and data to the memory device 100. During a read operation, the memory controller 200 may provide a read command and a physical block address (PBA) to the memory device 100. During an erase operation, the memory controller
10 200 may provide an erase command and a physical block address (PBA) to the memory device 100.

[0043] In an embodiment, the memory controller 200 may autonomously generate a command, an address, and data regardless of whether a request from the host is received, and may transmit them to the memory
15 device 100. For example, the memory controller 200 may provide commands, addresses, and data to the memory device 100 so as to perform background operations, such as a program operation for wear leveling and a program operation for garbage collection.

[0044] In an embodiment, the memory controller 200 may control at least
20 two memory devices 100. In this case, the memory controller 200 may control the memory devices 100 using an interleaving scheme to improve operating performance. The interleaving scheme may be an operating manner in which the operating periods of at least two memory devices 100 are caused to overlap each other.

[0045] The host may communicate with the storage device 50 using at least one of various communication methods such as Universal Serial Bus (USB), Serial AT Attachment (SATA), Serial Attached SCSI (SAS), High Speed Interchip (HSIC), Small Computer System Interface (SCSI), Peripheral Component Interconnection (PCI), PCI express (PCIe), Nonvolatile Memory express (NVMe), Universal Flash Storage (UFS), Secure Digital (SD), MultiMedia Card (MMC), embedded MMC (eMMC), Dual In-line Memory Module (DIMM), Registered DIMM (RDIMM), and Load Reduced DIMM (LRDIMM) communication methods.

10 **[0046]** FIG. 2 is a diagram illustrating the structure of the memory device of FIG. 1.

[0047] Referring to FIG. 2, the memory device 100 may include a memory cell array 110, a peripheral circuit 120, and control logic 130. The control logic 130 may be implemented as hardware, software, or a combination of hardware and software. For example, the control logic 130 may be a control logic circuit operating in accordance with an algorithm and/or a processor executing control logic code.

20 **[0048]** The memory cell array 110 includes a plurality of memory blocks BLK1 to BLKz. The plurality of memory blocks BLK1 to BLKz are coupled to an address decoder 121 through row lines RL. The memory blocks BLK1 to BLKz are coupled to a read and write circuit 123 through bit lines BL1 to BLm. Each of the memory blocks BLK1 to BLKz includes a plurality of memory cells. In an embodiment, the plurality of memory cells are nonvolatile memory cells. In the plurality of memory cells,

memory cells coupled to the same word line are defined as a single physical page. That is, the memory cell array 110 is composed of a plurality of physical pages. In accordance with an embodiment of the present disclosure, each of the plurality of memory blocks BLK1 to BLKz
5 included in the memory cell array 110 may include a plurality of dummy cells. As the dummy cells, one or more dummy cells may be coupled in series between a drain select transistor and the memory cells and between a source select transistor and the memory cells.

[0049] Each of the memory cells of the memory device 100 may be
10 implemented as a single-level cell (SLC) capable of storing a single data bit, a multi-level cell (MLC) capable of storing two data bits, a triple-level cell (TLC) capable of storing three data bits, or a quad-level cell (QLC) capable of storing four data bits.

[0050] The peripheral circuit 120 may include the address decoder 121, a
15 voltage generator 122, the read and write circuit 123, a data input/output circuit 124, and a sensing circuit 125.

[0051] The peripheral circuit 120 may generate control signals that control the memory cell array 10 to perform a program operation, a read operation, or an erase operation.

[0052] The address decoder 121 is coupled to the memory cell array 110
20 through row lines RL. The row lines RL may include drain select lines, word lines, source select lines, and a common source line. In accordance with an embodiment of the present disclosure, the word lines may include normal word lines and dummy word lines. In accordance with an

embodiment of the present disclosure, the row lines RL may further include a pipe select line.

[0053] In an embodiment, the row lines RL may be local lines included in local line groups. A local line group may correspond to a single memory
5 block. The local line group may include a drain select line, local word lines, and a source select line.

[0054] The address decoder 121 may be operated under the control of the control logic 130. The address decoder 121 receives addresses ADDR from the control logic 130.

10 **[0055]** The address decoder 121 may decode a block address among the received addresses ADDR. The address decoder 121 selects at least one memory block from among the memory blocks BLK1 to BLKz in response to the decoded block address. The address decoder 121 is configured to decode a row address RADD among the received addresses ADDR. The
15 address decoder 121 may select at least one word line of the selected memory block by applying voltages supplied from the voltage generator 122 to at least one word line WL in response to the decoded row address RADD.

[0056] During a program operation, the address decoder 121 may apply a
20 program voltage to the selected word line and apply a pass voltage having a level lower than that of the program voltage to unselected word lines. During a program verify operation, the address decoder 121 may apply a verify voltage to a selected word line and apply a verify pass voltage having a level higher than that of the verify voltage to unselected

word lines.

[0057] During a read operation, the address decoder 121 may apply a read voltage to a selected word line and apply a read pass voltage having a level higher than that of the read voltage to unselected word lines.

5 **[0058]** In accordance with an embodiment of the present disclosure, the erase operation of the memory device 100 may be performed on a memory block basis. During an erase operation, the addresses ADDR input to the memory device 100 include a block address. The address decoder 121 may decode the block address and select a single memory
10 block in response to the decoded block address. During the erase operation, the address decoder 121 may apply a ground voltage to word lines coupled to the selected memory block.

[0059] In accordance with an embodiment of the present disclosure, the address decoder 121 may decode a column address among the received
15 addresses ADDR. The decoded column address may be transferred to the read and write circuit 123. In an embodiment, the address decoder 121 may include components such as a row decoder, a column decoder, and an address buffer.

[0060] The voltage generator 122 may generate a plurality of operating
20 voltages V_{op} using an external supply voltage that is supplied to the memory device 100. The voltage generator 122 may be operated under the control of the control logic 130.

[0061] In an embodiment, the voltage generator 122 may generate an internal supply voltage by regulating the external supply voltage. The

internal supply voltage generated by the voltage generator 122 is used as an operating voltage for the memory device 100.

[0062] In an embodiment, the voltage generator 122 may generate the plurality of operating voltages Vop using the external supply voltage or the internal supply voltage. The voltage generator 122 may generate various voltages required by the memory device 100. For example, the voltage generator 122 may generate a plurality of erase voltages, a plurality of program voltages, a plurality of pass voltages, a plurality of select read voltages, and a plurality of unselect read voltages.

[0063] The voltage generator 122 may include a plurality of pumping capacitors for receiving the internal supply voltage so as to generate a plurality of operating voltages Vop having various voltage levels, and may generate the plurality of operating voltages Vop by selectively enabling the plurality of pumping capacitors under the control of the control logic 130.

[0064] The generated operating voltages Vop may be supplied to the memory cell array 110 by the address decoder 121.

[0065] The read and write circuit 123 includes first to m-th page buffers PB1 to PBm. The first to m-th page buffers PB1 to PBm are coupled to the memory cell array 110 through the first to m-th bit lines BL1 to BLm, respectively. The first to m-th page buffers PB1 to PBm are operated under the control of the control logic 130.

[0066] The first to m-th page buffers PB1 to PBm perform data communication with the data input/output circuit 124. During a program

operation, the first to m-th page buffers PB1 to PBm receive data DATA to be stored through the data input/output circuit 124 and data lines DL.

5 **[0067]** During a program operation, the first to m-th page buffers PB1 to PBm may transfer the data DATA to be stored, received through the data input/output circuit 124, to selected memory cells through the bit lines BL1 to BLm when a program pulse is applied to a selected word line. Memory cells in a selected page are programmed based on the received data DATA. Memory cells coupled to a bit line to which a program permission voltage (e.g., a ground voltage) is applied may have increased
10 threshold voltages. The threshold voltages of memory cells coupled to a bit line to which a program inhibit voltage (e.g., a supply voltage) is applied may be maintained. During a program verify operation, the first to m-th page buffers PB1 to PBm read the data DATA stored in the selected memory cells from the selected memory cells through the bit
15 lines BL1 to BLm.

[0068] During a read operation, the read and write circuit 123 may read data DATA from the memory cells in the selected page through the bit lines BL, and may store the read data DATA in the first to m-th page buffers PB1 to PBm.

20 **[0069]** During an erase operation, the read and write circuit 123 may allow the bit lines BL to float. In an embodiment, the read and write circuit 123 may include a column select circuit.

[0070] In an embodiment, the read and write circuit 123 may include the plurality of page buffers PB coupled to the memory cells of the memory

cell array 110 through the bit lines BL.

[0071] The plurality of page buffers PB may be divided into a plurality of page buffer groups. The bit lines BL may be divided into a plurality of bit line groups respectively corresponding to the plurality of page buffer groups. The plurality of page buffer groups may perform bit line precharge operations of precharging the plurality of bit line groups corresponding thereto, respectively, during a program operation performed on the memory cells.

[0072] Read and write circuit control signals PBSIGNALS may include a plurality of page buffer control signals respectively corresponding to the plurality of page buffer groups. The plurality of page buffer groups may independently perform bit line precharge operations in response to the plurality of page buffer control signals corresponding thereto, respectively. The coupling relationships between the plurality of page buffer groups and the memory cells will be described with reference to FIG. 9.

[0073] The data input/output circuit 124 is coupled to the first to m-th page buffers PB1 to PBm through the data lines DL. The data input/output circuit 124 is operated in response to the control of the control logic 130.

[0074] The data input/output circuit 124 may include a plurality of input/output buffers (not illustrated) which receive input data DATA. During a program operation, the data input/output circuit 124 receives the data DATA to be stored from an external controller (not illustrated). During a read operation, the data input/output circuit 124 outputs the

data DATA, received from the first to m-th page buffers PB1 to PBm included in the read and write circuit 123, to the external controller.

[0075] During a read operation or a verify operation, the sensing circuit 125 may generate a reference current in response to an enable bit signal VRYBIT generated by the control logic 130, and may output a pass signal or a fail signal to the control logic 130 by comparing a sensing voltage VPB received from the read and write circuit 123 with a reference voltage generated by the reference current.

[0076] The control logic 130 may be coupled to the address decoder 121, the voltage generator 122, the read and write circuit 123, the data input/output circuit 124, and the sensing circuit 125. The control logic 130 may control the overall operation of the memory device 100. The control logic 130 may be operated in response to a command CMD transmitted from an external device.

[0077] The control logic 130 may control the peripheral circuit 120 by generating various types of signals in response to the command CMD and the addresses ADDR. For example, the control logic 130 may generate an operation signal OPSIG, a row address RADD, a page buffer control signal PBSIGNALS, and an enable bit VRYBIT in response to the command CMD and the addresses ADDR. The control logic 130 may output the operation signal OPSIG to the voltage generator 122, output the row address RADD to the address decoder 121, output the page buffer control signal PBSIGNALS to the read and write circuit 123, and output the enable bit VRYBIT to the sensing circuit 125. In addition, the control

logic 130 may determine whether a verify operation has passed or failed in response to the pass or fail signal PASS or FAIL output from the sensing circuit 125.

5 **[0078]** In an embodiment, the control logic 130 may include a program operation controller 131.

[0079] The program operation controller 131 may control the plurality of page buffer groups included in the read and write circuit 123 so that the respective page buffer groups initiate bit line precharge operations at different time points.

10 **[0080]** For example, the program operation controller 131 may provide the read and write circuit control signals PBSIGNALS, including the plurality of page buffer control signals respectively corresponding to the plurality of page buffer groups, to the read and write circuit 123. The plurality of page buffer groups may independently perform bit line precharge
15 operations in response to the plurality of page buffer control signals corresponding thereto, respectively.

[0081] The program operation controller 131 may adjust an interval between the initiation time points of the bit line precharge operations performed by respective page buffer groups depending on the progress of
20 the program operation.

[0082] The progress of the program operation may be determined to be a highest program state, among program states for which a program verify operation has passed. Alternatively, the progress of the program operation may be determined to be a program loop count indicating the

number of program loops that have been performed, among one or more program loops that are performed during the program operation.

[0083] FIG. 3 is a diagram illustrating the memory cell array of FIG. 2.

[0084] Referring to FIG. 3, the first to z-th memory blocks BLK1 to BLKz are coupled in common to the first to m-th bit lines BL1 to BLm. In FIG. 3, for convenience of description, elements included in the first memory block BLK1, among the plurality of memory blocks BLK1 to BLKz, are illustrated, and illustration of elements included in each of the remaining memory blocks BLK2 to BLKz is omitted. It will be understood that each of the remaining memory blocks BLK2 to BLKz has the same configuration as the first memory block BLK1.

[0085] The memory block BLK1 may include a plurality of cell strings CS1_1 to CS1_m (where m is a positive integer). The first to m-th cell strings CS1_1 to CS1_m are respectively coupled to the first to m-th bit lines BL1 to BLm. Each of the first to m-th cell strings CS1_1 to CS1_m may include a drain select transistor DST, a plurality of memory cells MC1 to MCn (where n is a positive integer) which are coupled in series to each other, and a source select transistor SST.

[0086] A gate terminal of the drain select transistor DST included in each of the first to m-th cell strings CS1_1 to CS1_m is coupled to a drain select line DSL1. Gate terminals of the first to n-th memory cells MC1 to MCn included in each of the first to m-th cell strings CS1_1 to CS1_m are coupled to first to n-th word lines WL1 to WLn, respectively. A gate terminal of the source select transistor SST included in each of the first to

m-th cell strings CS1_1 to CS1_m is coupled to a source select line SSL1.

[0087] For convenience of description, the structure of each cell string will be described based on the first cell string CS1_1, among the plurality of cell strings CS1_1 to CS1_m. However, it will be understood that each of
5 the remaining cell strings CS1_2 to CS1_m is configured in the same manner as the first cell string CS1_1.

[0088] A drain terminal of the drain select transistor DST included in the first cell string CS1_1 is coupled to the first bit line BL1. A source terminal of the drain select transistor DST included in the first cell string
10 CS1_1 is coupled to a drain terminal of the first memory cell MC1 included in the first cell string CS1_1. The first to n-th memory cells MC1 to MCn may be coupled in series to each other. A drain terminal of the source select transistor SST included in the first cell string CS1_1 is coupled to a source terminal of the n-th memory cell MCn included in the first cell
15 string CS1_1. A source terminal of the source select transistor SST included in the first cell string CS1_1 is coupled to a common source line CSL. In an embodiment, the common source line CSL may be coupled in common to the first to z-th memory blocks BLK1 to BLKz.

[0089] The drain select line DSL1, the first to n-th word lines WL1 to WLn,
20 and the source select line SSL1 are included in the row lines RL of FIG. 2. The drain select line DSL1, the first to n-th word lines WL1 to WLn, and the source select line SSL1 are controlled by the address decoder 121. The common source line CSL is controlled by the control logic 130. The first to m-th bit lines BL1 to BLm are controlled by the read and write

circuit 123.

[0090] FIG. 4 is a diagram illustrating a program operation according to an embodiment.

[0091] Referring to FIG. 4, the program operation may include a plurality
5 of program loops PL1 to PLn. The memory device may perform a program operation so that each of selected memory cells has any one of a plurality of program states by performing the plurality of program loops PL1 to PLn.

[0092] Each of the plurality of program loops PL1 to PLn may include a
10 program voltage apply step (PGM step) of applying a program voltage and a verify step of verifying whether the memory cells have been programmed by applying verify voltages.

[0093] At the program voltage apply step, a program voltage apply operation of applying the program voltage to a selected word line coupled
15 to the selected memory cells may be performed. Each of the selected memory cells may be programmed to a program state corresponding to any one of first to n-th states (where n is a natural number) through the program voltage apply operation.

[0094] In an embodiment, the program voltage may be determined based
20 on an incremental step pulse programming (ISPP) method. That is, the level of the program voltage may be increased or decreased by a predetermined voltage increment (i.e., a step voltage) in a step-by-step manner while the program loops are repeated. The number of applications of program voltages used in respective program loops, the

voltage levels of the program voltages, voltage application times, etc. may be determined in various forms under the control of the memory controller.

[0095] A pass voltage may be applied to the remaining word lines, that is, 5 unselected word lines, other than the selected word line. In an embodiment, pass voltages having the same level may be applied to the unselected word lines. In an embodiment, the pass voltage may have different levels depending on the locations of word lines.

[0096] A ground voltage may be applied as a program permission voltage 10 to the selected bit lines coupled to the memory cells to be programmed. A program inhibition voltage may be applied to the unselected bit lines, which are bit lines coupled to memory cells other than the memory cells to be programmed.

[0097] The memory device may apply the verify voltages to the selected 15 word line and apply a verify pass voltage to the unselected word lines at the program verify step. The memory device may sense voltages or currents output through the bit lines to which the memory cells coupled to the selected word line are respectively coupled, and may determine whether the verify step has passed or failed based on the results of 20 sensing.

[0098] At the verify step, a program verify operation may be performed for at least one of the first to n-th program states. For example, when memory cells to be programmed to a k-th state (where k is a natural number that is equal to or greater than 1 and is less than or equal to n)

are read as off-cells through the verify voltage corresponding to the k-th state, a program verify operation for the k-th state may pass.

[0099] In FIG. 4, when the selected memory cells are multi-level cells (MLC), each storing two data bits, the selected memory cells may be programmed to any one of an erased state and first to third program states. The number of data bits stored in one memory cell is not limited to the present embodiments.

[00100] When the first program loop PL1 is performed, a first program voltage V_{pgm1} is applied, and thereafter the first to third verify voltages V_{vfy1} to V_{vfy3} are sequentially applied so as to verify the program states of the plurality of memory cells. Here, memory cells, the target states of which are the first program state, may be verified using the first verify voltage V_{vfy1} , memory cells, the target states of which are the second program state, may be verified using the second verify voltage V_{vfy2} , and memory cells, the target states of which are the third program state, may be verified using the third verify voltage V_{vfy3} . The number of verify voltages is not limited to the present embodiments.

[00101] The memory cells which have passed verification through respective verify voltages V_{vfy1} to V_{vfy3} may be determined to have the target states, and may then be program inhibited in the second program loop PL2. A program inhibition voltage may be applied to the bit lines coupled to the program-inhibited memory cells. In the second program loop PL2, a second program voltage V_{pgm2} higher than the first program voltage V_{pgm1} by a unit voltage ΔV_{pgm} is applied to the

selected word line.

[00102] Thereafter, a verify operation is performed in the same way as the verify operation in the first program loop PL1. In an example, the term "verification pass" indicates that each memory cell is read as an off-cell through the corresponding verify voltage.

[00103] As described above, when the memory device programs multi-level cells (MLC), the memory device verifies the memory cells having respective program states as target states using the first to third verify voltages V_{vfy1} to V_{vfy3} .

[00104] In various embodiments, when the program operation is not completed within a preset number of program loops, the program operation may fail. When the program operation is completed within a preset number of program loops, the program operation may pass. Whether the program operation is completed may be determined depending on whether the selected memory cells have passed all program verify operations.

[00105] In an embodiment, one or more program loops may be performed during the program operation. The progress of the program operation may indicate program loops which have been completed up to a current time, among all program loops, during the program operation. That is, the progress of the program operation may be a program loop count indicating the number of program loops that have been performed, among one or more program loops.

[00106] FIG. 5 is a diagram illustrating a progress sequence of a

program operation according to an embodiment.

[00107] Referring to FIG. 5, a description will be made on the assumption that each memory cell is a quad-level cell (QLC) which stores four data bits. Each memory cell may be programmed to any one of an
5 erased state E and first to fifteenth program states P1 to P15.

[00108] The memory cell may store logical data corresponding to any one of the erased state E and the plurality of program states P1 to P15. The logical data may include Upper Significant Bit (USB) page data, Most Significant Bit (MSB) page data, Central Significant Bit (CSB) page data,
10 and Least Significant Bit (LSB) page data.

[00109] In FIG. 5, the erased state E and the first to fifteenth program states P1 to P15 may correspond to pieces of logical data '1111', '1110', '1100', '1000', '0000', '0100', '0101', '0111', '0110', '0010', '1010', '1011', '0011', '0001', '1001' and '1101', respectively. The pieces of
15 logical data corresponding to respective states are not limited to the present embodiments.

[00110] The program operation may be sequentially performed in a sequence from the first program state P1 to the fifteenth program state P15. A program verify operation may also be sequentially performed in a
20 sequence from a program verify operation for the first program state P1 to a program verify operation for the fifteenth program state P15.

[00111] The progress of the program operation may indicate a point up to which the program operation has been completed within a range from a start point to an end point. In an embodiment, the progress of

the program operation may be a highest program state, among states for which the program verify operation has passed.

[00112] For example, when program verify operations for the first to fifth program states P1 to P5 have passed and program verify operations for the remaining program states P6 to P15 have failed, the progress of the program operation may correspond to the fifth program state P5. It can be seen that, by means of the progress of the program operation, the program operation for the first to fifth program states P1 to P5, among all of the program states P1 to P15, has been completed.

[00113] FIG. 6 is a diagram for explaining bit line loading.

[00114] Referring to FIG. 6, a program permission voltage may be applied to bit lines coupled to cells to be programmed. In an embodiment, the program permission voltage may be a ground voltage V_{gnd} .

[00115] A program inhibition voltage V_{inh} may be applied to bit lines coupled to cells for which programming has been completed. In an embodiment, the program inhibition voltage may be a supply voltage.

[00116] At a start point of the program operation PGM Start, first to eighth bit lines BL1 to BL8 may be bit lines coupled to cells to be programmed.

[00117] While the program operation is performed (Programming), the first, third, fifth, and eighth bit lines BL1, BL3, BL5, and BL8 may be bit lines coupled to cells to be programmed. The second, fourth, sixth, and seventh bit lines BL2, BL4, BL6, and BL7 may be bit lines coupled to

cells for which programming has been completed.

[00118] At an end point of the program operation PGM End, the first to eighth bit lines BL1 to BL8 may be bit lines coupled to cells for which programming has been completed.

5 **[00119]** Bit line loading may occur due to capacitance between adjacent bit lines. The bit line loading may be a burden required to precharge the bit lines to a certain level. Thus, a value of the bit line loading may be measured in various ways. In an embodiment, the bit line loading may be caused by the capacitance between the adjacent bit lines
10 and may be proportional to the capacitance. Thus, the value of the bit line loading may be measured by a value of the capacitance. In an embodiment, the value of the bit line loading may be measured by a time to precharge the bit lines to a certain level when the other conditions are same. In an embodiment, the value of the bit line loading may be
15 measured by power required to precharge the bit lines to a certain level when the other conditions are same. In an embodiment, the value of the bit line loading may be used as a relative measure for comparing. Thus, the value of the bit line loading does not have specific unit.

[00120] The magnitude of the capacitance may be proportional to the
20 difference between voltages applied to the adjacent bit lines. Therefore, when the voltage difference between the adjacent bit lines is large, bit line loading may have a large value, whereas when the voltage difference between the adjacent bit lines is small, bit line loading may have a small value.

[00121] As a bit line loading value is larger, a longer time may be required in order to perform a bit line precharge operation of increasing the potentials of the bit lines to a certain level. As a bit line loading value is smaller, a shorter time may be required in order to perform the bit line precharge operation.

[00122] In FIG. 6, since the voltages of the adjacent bit lines at the start point of the program operation PGM Start are identical to each other and are the ground voltage V_{gnd} , which is the program permission voltage, a bit line loading value may be small. Therefore, during the bit line precharge operation, a shorter time may be required.

[00123] While the program operation is performed (Programming), the bit lines coupled to the cells to be programmed and the bit lines coupled to the cells for which programming has been completed may be adjacent to each other. Therefore, since the voltages of the adjacent bit lines are different from each other, a voltage difference may occur, and bit line loading may be large. Therefore, a longer time may be required for the bit line precharge operation.

[00124] Since the voltages of the adjacent bit lines at the end point of the program operation PGM End are equal to each other as the program inhibition voltage V_{inh} , bit line loading may be small. Therefore, a shorter time may be required for the bit line precharge operation.

[00125] FIG. 7 is a diagram for explaining a change in bit line loading depending on the progress of a program operation.

[00126] Referring to FIG. 7, a horizontal axis of the graph may

indicate time, and a vertical axis of the graph may indicate bit line loading.

[00127] At a start point of a program operation PGM Start, bit lines may be bit lines coupled to cells to be programmed. Therefore, since there are many cases where the voltages of adjacent bit lines are equal to each other as a program permission voltage at the start point of the program operation PGM Start, bit line loading may be small.

[00128] At a middle point of the program operation PGM Mid, the number of bit lines coupled to cells to be programmed may be similar to the number of bit lines coupled to cells for which programming has been completed. Therefore, in the largest number of cases, the voltages of the adjacent bit lines are different from each other as the program permission voltage and the program inhibition voltage, respectively, and thus bit line loading may be the largest.

[00129] At an end point of the program operation PGM End, bit lines may be bit lines coupled to cells for which programming has been completed. Therefore, since there are many cases where the voltages of adjacent bit lines are equal to each other as the program inhibition voltage at the end point of the program operation PGM End, bit line loading may be small.

[00130] While the program operation is performed, the number of bit lines coupled to cells to be programmed, among all bit lines, may decrease, and the number of bit lines coupled to cells for which programming has been completed may increase.

[00131] Therefore, since the number of cases where the voltages of

adjacent bit lines are different from each other as the program permission voltage and the program inhibition voltage, respectively, may increase in a range from the start point of the program operation PGM Start to the middle point of the program operation PGM Mid, bit line loading may increase. Since the number of cases where the voltages of adjacent bit lines are different from each other decreases in a range from the middle point of the program operation (PGM Mid) to the end point of the program operation (PGM End), bit line loading may decrease.

[00132] In an embodiment, the memory device may predict a change in bit line loading based on the progress of the program operation. The memory device may determine the time required for the bit line precharge operation depending on the change in bit line loading. Therefore, the memory device may set the time required for the bit line precharge operation to different times depending on the progress of the program operation.

[00133] For example, the memory device may set the time required for the bit line precharge operation when the progress of the program operation exists between a point t_a and a point t_b to a time longer than that when the progress of the program operation exists between the start point of the program operation PGM Start and the point t_a . The memory device may set the time required for the bit line precharge operation when the progress of the program operation exists between the point t_a and the point t_b to a time longer than that when the progress of the program operation exists between the point t_b and the end point of the

program operation PGM End.

[00134] As will be described later with reference to FIGS. 12 and 13, the memory device may adjust the interval between initiation time points of respective bit line precharge operations of page buffer groups in order to set the time required for the entire bit line precharge operation to different times. For example, the memory device may increase the interval between the initiation time points of respective bit line precharge operations of the page buffer groups in order to set the time required for the entire bit line precharge operation to a longer time. The memory device may decrease the interval between the initiation time points of respective bit line precharge operations of the page buffer groups in order to set the time required for the entire bit line precharge operation to a shorter time.

[00135] The memory device may adjust the interval between the initiation time points of respective bit line precharge operations of the plurality of page buffer groups based on the progress of the program operation and the results of a comparison between values at one or more reference points.

[00136] In FIG. 7, the points t_a and t_b may be reference points based on which the time required for the corresponding bit line precharge operation is set to different times.

[00137] In an embodiment, when the progress of the program operation is a program loop count, described above with reference to FIG. 4, the reference points may correspond to reference values. For example,

assuming that a program loop is performed 100 times during the program operation, a reference value at the point ta may be 25 (times), a reference value at the middle point of the program operation PGM Mid may be 50 (times), and a reference value at the point tb may be 75 (times).

5 [00138] When the program loop count is equal to or greater than 25 that is the reference value at the point ta, the memory device may increase the interval between the initiation time points of respective bit line precharge operations of the page buffer groups in order to set the
10 time required for the entire bit line precharge operation to a long time. When the program loop count is equal to or greater than 75 that is the reference value at the point tb, the memory device may decrease the interval between the initiation time points of respective bit line precharge operations of the page buffer groups in order to set the time required for
15 the entire bit line precharge operation to a short time.

[00139] In an embodiment, when the progress of the program operation is the highest program state for which the program verify operation, described above with reference to FIG. 5, has passed, the reference point may correspond to a reference state. For example, when
20 the program operation starts at the erased state E and is then performed up to a fifteenth program state P15, the reference state at the point ta may be a third program state P3, the reference state at the middle point of the program operation PGM Mid may be a seventh state P7, and the reference state at the point tb may be an eleventh program state P11.

[00140] When the highest program state for which the program verify operation has passed is equal to or higher than the third program state P3 that is the reference state at the point ta, the memory device may increase the interval between the initiation time points of respective
5 bit line precharge operations of the page buffer groups in order to set the time required for the entire bit line precharge operation to a longer time. When the highest program state for which the program verify operation has passed is equal to or higher than the eleventh program state P11 that is the reference state at the point tb, the memory device may decrease
10 the interval between the initiation time points of respective bit line precharge operations of the page buffer groups in order to set the time required for the entire bit line precharge operation to a shorter time.

[00141] In various embodiments, the program operation may be divided into a plurality of periods depending on the plurality of points.
15 The memory device may set times required for bit line precharge operations in respective periods to different times based on the bit line loading values of respective periods. The memory device may adjust the interval between the initiation time points of bit line precharge operations in respective periods based on the bit line loading values of respective
20 periods.

[00142] In accordance with an embodiment of the present disclosure, the time required for the entire bit line precharge operation may be set in consideration of bit line loading depending on the progress of the program operation. For example, in order to set the time required for the entire

bit line precharge operation, the interval between the initiation time points of respective bit line precharge operations performed by the plurality of page buffer groups may be adjusted.

[00143] In this way, the time required for the bit line precharge operation during a period in which bit line loading is small may be shortened, and the speed of the entire program operation may be improved.

[00144] FIG. 8 is a diagram illustrating the configuration and operation of a memory device according to an embodiment.

[00145] Referring to FIG. 8, a memory cell array 110 may include a plurality of memory cells. A read and write circuit 123 may include a plurality of page buffer groups PBG1 to PBG4.

[00146] The plurality of memory cells may be coupled to the plurality of page buffer groups PBG1 to PBG4 of the read and write circuit 123 through a plurality of bit line groups BLGs.

[00147] The plurality of page buffer groups PBG1 to PBG4 may respectively perform bit line precharge operations of precharging the corresponding bit line groups BLGs. The page buffer groups PBG1 to PBG4 may perform respective bit line precharge operations in response to a plurality of page buffer control signals included in read and write circuit control signals PBSIGNALS. For example, each page buffer group may perform a bit line precharge operation during a period in which the corresponding page buffer control signal is activated.

[00148] The plurality of page buffer groups PBG1 to PBG4 may

initiate bit line precharge operations at different time points. The lengths of the periods of the bit line precharge operations performed by respective page buffer groups PBG1 to PBG4 may differ from each other. Alternatively, the lengths of the periods of the bit line precharge operations performed by respective page buffer groups PBG1 to PBG4 may be equal to each other.

[00149] The program operation controller 131 may include a program loop counter 131a, a program state determiner 131b, and a page buffer controller 131c.

10 **[00150]** The program loop counter 131a may count the number of program loops which have been performed, among one or more program loops which are to be performed during a program operation. The program loop counter 131a may generate program loop count information PL_INF indicating a program loop count that is the number of program loops which have been performed. The program loop counter 131a may provide the generated program loop count information PL_INF to the page buffer controller 131c.

20 **[00151]** The program state determiner 131b may determine the highest program state, among program states for which a program verify operation has passed, during the program operation. The program state determiner 131b may generate program state information PV_INF indicating the highest program state, among the program states for which the program verify operation has passed. The program state determiner 131b may provide the generated program state information PV_INF to the

page buffer controller 131c.

[00152] The page buffer controller 131c may provide the read and write circuit control signals PBSIGNALS to the read and write circuit 123. The read and write circuit control signals PBSIGNALS may include a plurality of page buffer control signals respectively corresponding to the plurality of page buffer groups PBG1 to PBG4.

[00153] The page buffer controller 131c may adjust the lengths of the periods of the bit line precharge operations of the page buffer groups in response to the page buffer control signals. The page buffer controller 131c may adjust the initiation time points of the bit line precharge operations of the page buffer groups in response to the page buffer control signals. For example, the page buffer controller 131c may apply an activated page buffer control signal to the page buffer group so that the corresponding page buffer group initiates the bit line precharge operation. The page buffer controller 131c may apply a deactivated buffer control signal to the page buffer group so that the corresponding page buffer group terminates the bit line precharge operation.

[00154] The page buffer controller 131c may control the plurality of page buffer groups PBG1 to PBG4 so that the page buffer groups PBG1 to PBG4 respectively perform bit line precharge operations in response to the plurality of page buffer control signals. The page buffer controller 131c may control the plurality of page buffer groups PBG1 to PBG4 so that the page buffer groups PBG1 to PBG4 respectively initiate bit line precharge operations at different time points.

[00155] In an embodiment, the page buffer controller 131c may adjust the interval between the initiation time points of the bit line precharge operations performed by respective page buffer groups PBG1 to PBG4 depending on the progress of the program operation. For example,
5 the page buffer controller 131c may adjust the interval between time points at which a plurality of page buffer control signals that are applied to the respective page buffer groups PBG1 to PBG4 are activated depending on the progress of the program operation.

[00156] In an embodiment, the page buffer controller 131c may
10 determine the progress of the program operation based on the program loop count contained in the program loop count information PL_INF.

[00157] The page buffer controller 131c may adjust the interval between the initiation time points of the bit line precharge operations based on the results of a comparison between the program loop count
15 and one or more reference values. The page buffer controller 131c may increase the interval between the initiation time points of the bit line precharge operations when the program loop count is equal to or greater than a first reference value. The page buffer controller 131c may decrease the interval between the initiation time points of the bit line
20 precharge operations when the program loop count is equal to or greater than a second reference value. The second reference value may be different from the first reference value. The second reference value may be greater than the first reference value.

[00158] In an embodiment, the page buffer controller 131c may

determine the progress of the program operation based on the highest program state for which a program verify operation has passed and which is contained in the program state information PV_INF.

[00159] The page buffer controller 131c may adjust the interval
5 between the initiation time points of the bit line precharge operations based on the results of a comparison between the highest program state and one or more reference states. The page buffer controller 131c may increase the interval between the initiation time points of the bit line precharge operations when the highest program state is equal to or
10 higher than a first reference state. The page buffer controller 131c may decrease the interval between the initiation time points of the bit line precharge operations when the highest program state is equal to or higher than a second reference state. The second reference state may be different from the first reference state. The second reference state
15 may be higher than the first reference state.

[00160] FIG. 9 is a diagram illustrating the read and write circuit of FIG. 8.

[00161] Referring to FIG. 9, the read and write circuit may include first to fourth page buffer groups PBG1 to PBG4. The number of page
20 buffer groups included in the read and write circuit is not limited to the present embodiments.

[00162] The unit of data stored in memory cells coupled to a single word line WL may be a page. Each page may include first to fourth sub-pages S1 to S4. The number of sub-pages included in each page is not

limited to the present embodiments.

[00163] Memory cells constituting each sub-page may be coupled to the corresponding page buffer group through the corresponding bit line group. For example, memory cells constituting a first sub-page S1 may be coupled to the first page buffer group PBG1 through a first bit line group BLG1. Memory cells constituting a second sub-page S2 may be coupled to the second page buffer group PBG2 through a second bit line group BLG2. Memory cells constituting a third sub-page S3 may be coupled to the third page buffer group PBG3 through a third bit line group BLG3. Memory cells constituting a fourth sub-page S4 may be coupled to the fourth page buffer group PBG4 through a fourth bit line group BLG4.

[00164] Each page buffer group may perform a bit line precharge operation of precharging the bit line group coupled thereto in response to an applied page buffer control signal. When an activated page buffer control signal is applied, each page buffer group may initiate a bit line precharge operation, whereas when a deactivated page buffer control signal is applied, each page buffer group may terminate the bit line precharge operation.

[00165] For example, the first page buffer group PBG1 may perform a bit line precharge operation of precharging the first bit line group BLG1 in response to a first page buffer control signal PBSense1. Similarly, the second to fourth page buffer groups PBG2 to PBG4 may respectively perform bit line precharge operations of precharging the corresponding second to fourth bit line groups BLG2 to BLG4 in response to the

corresponding second to fourth page buffer control signals PBSENSE2 to PBSENSE4.

[00166] FIG. 10 is a diagram illustrating the program voltage apply step of FIG. 4.

5 **[00167]** Referring to FIG. 10, the program voltage apply step may include a bit line precharge operation, a bit line floating operation, and a program voltage apply operation.

[00168] During a period from a time point t1 to a time point t3, a bit line precharge operation of precharging the potential of the corresponding
10 bit line to a certain level may be performed to perform a program operation.

[00169] During the period from the time point t1 to the time point t3, a page buffer control signal PBSENSE may be activated. For example, at the time point t1, the page buffer control signal PBSENSE may make a
15 transition from a low level to the level of a control voltage VPB and then be activated. At the time point t3, the page buffer control signal PBSENSE may make a transition from the level of the control voltage VPB to a low level and then be deactivated.

[00170] In an embodiment, when the activated page buffer control
20 signal PBSENSE is applied to the page buffer group, the page buffer group may initiate the bit line precharge operation. When the deactivated page buffer control signal PBSENSE is applied to the page buffer group, the page buffer group may terminate the bit line precharge operation.

[00171] During the activation of the page buffer control signal

PBSENSE, the bit line precharge operation may be performed while a program permission voltage V_{gnd} or a program inhibition voltage V_{inh} is applied to the bit lines.

[00172] For example, during the activation of the page buffer control signal PBSENSE, the program permission voltage V_{gnd} may be applied to a bit line PGM BL coupled to a cell to be programmed. In an embodiment, the program permission voltage V_{gnd} may be a ground voltage. The program inhibition voltage V_{inh} may be applied to a bit line coupled to a program-inhibited cell, that is, Inhibit BL. In an embodiment, the program inhibition voltage V_{inh} may be a supply voltage.

[00173] At the time point t_3 , the potential of the bit line PGM BL may be set to the ground voltage, and the potential of the bit line Inhibit BL may be set to the program inhibition voltage V_{inh} .

[00174] The bit line floating operation of maintaining the potential of the precharged bit line may be performed during a period from the time point t_3 to a time point t_6 .

[00175] During the period from the time point t_3 to the time point t_6 , the page buffer control signal PBSENSE may be deactivated. For example, at the time point t_3 , the page buffer control signal PBSENSE may make a transition from the level of the control voltage V_{PB} to a low level and then be deactivated.

[00176] When the page buffer control signal PBSENSE is deactivated, the bit line may float, and the potential of the bit line may be maintained at the precharged voltage level.

[00177] During the period from the time point t3 to the time point t6, the potential of the bit line PGM BL may be maintained at the ground voltage, and the potential of the bit line Inhibit BL may be maintained at the program inhibition voltage Vinh.

5 **[00178]** During a period from a time point t4 to the time point t6, the program voltage Vpgm apply operation of applying a program voltage Vpgm to a selected word line Sel.WL may be performed. For example, a pass voltage Vpass may be first applied to the selected word line Sel.WL and an unselected word line (not illustrated). Thereafter, the program
10 voltage Vpgm may be applied to the selected word line Sel.WL.

[00179] During the period from the time point t4 to the time point t6, the potential of the selected word line Sel.WL may increase up to the pass voltage Vpass, and may then increase up to the program voltage Vpgm. The potential of the unselected word line may increase up to the pass
15 voltage Vpass, and may then be maintained at the pass voltage Vpass.

[00180] In FIG. 10, whether to perform a program operation on the corresponding memory cell may be determined depending on the difference between the program voltage Vpgm applied to the selected word line and a bit line voltage applied to the bit line.

20 **[00181]** The potential difference between the program permission voltage Vgnd and the program voltage Vpgm may be sufficient to perform a program operation. Therefore, the memory cell coupled to the bit line PGM BL precharged to the program permission voltage Vgnd may be programmed.

[00182] The potential difference between the program inhibition voltage V_{inh} and the program voltage V_{pgm} may be insufficient to perform a program operation. Therefore, the memory cell coupled to the bit line Inhibit BL precharged to the program inhibition voltage V_{inh} may not be programmed.

[00183] FIG. 11 is a diagram illustrating a bit line precharge operation according to an embodiment.

[00184] Referring to FIGS. 9 and 11, a plurality of page buffer control signals $PBSENSE1$ to $PBSENSE4$ respectively corresponding to a plurality of page buffer groups $PBG1$ to $PBG4$ may be applied to the page buffer groups $PBG1$ to $PBG4$.

[00185] In FIG. 11, the plurality of page buffer control signals $PBSENSE1$ to $PBSENSE4$ may be identical to each other as a page buffer control signal $PBSENSE$. That is, the same page buffer control signal $PBSENSE$ may be applied to all of the plurality of page buffer groups All PBG.

[00186] During a period from a time point $ta1$ to a time point $ta2$, the page buffer control signal $PBSENSE$ having a constant slope may be applied to all of the plurality of page buffer groups All PBG.

[00187] For example, during the period from the time point $ta1$ to the time point $ta2$, the page buffer control signal $PBSENSE$ may increase from a low level to the level of the control voltage VPB while having a constant slope.

[00188] During a period from the time point $ta2$ to a time point $ta3$,

the page buffer control signal PBSENSE having the level of the control voltage VPB may be applied to all of the plurality of page buffer groups All PBG.

[00189] Depending on the level of the page buffer control signal
5 PBSENSE, the magnitude of a voltage that is transferred to the bit line may be adjusted. As the level of the page buffer control signal PBSENSE becomes higher, the magnitude of the voltage that is transferred to the bit line may increase, and thus the bit line precharge speed may increase. However, as the bit line precharge speed becomes higher, the quantity of
10 electric charge stored for the same time may increase, and thus the amount of peak current generated in each page buffer group may also increase.

[00190] During an initial period of the bit line precharge operation in which the potential of each bit line rapidly increases, power consumption
15 may be high, and during the latter period of the bit line precharge operation in which the potential of the bit line gently increases, power consumption may be low.

[00191] In the case of the bit line precharge operation of FIG. 10, the page buffer control signal PBSENSE may make a rapid transition from the
20 low level to the level of the control voltage VPB at the time point t1, and may be maintained at the level of the control voltage VPB during the period from the time point t1 to the time point t3.

[00192] As illustrated in FIG. 10, when the page buffer control signal PBSENSE having the level of the control voltage VPB is applied to all of

the plurality of page buffer groups All PBG during the initial period from t1 to t2 of the bit line precharge operation, power consumption of all of the plurality of page buffer groups All PBG may rapidly increase, and thus a peak current exceeding a threshold value may be generated.

5 **[00193]** In the case of the bit line precharge operation of FIG. 11, the page buffer control signal PBSENSE may make a gentle transition from the low level to the level of the control voltage VPB while having a constant slope during the period from the time point ta1 to the time point ta2. The page buffer control signal PBSENSE may be maintained at the
10 level of the control voltage VPB during a period from the time point ta2 to the time point ta3.

[00194] As illustrated in FIG. 11, when the page buffer control signal PBSENSE having a constant slope is applied to all of the plurality of page buffer groups All PBG during the initial period from ta1 to ta2 of the bit
15 line precharge operation, power consumption of all of the plurality of page buffer groups All PBG may gently increase, and thus the generation of a peak current exceeding a threshold value may be prevented.

[00195] In various embodiments, the value of the slope may be adjusted to prevent the generation of a peak current.

20 **[00196]** As the value of the slope is smaller, generation of a peak current may be more effectively prevented. However, the value of the slope may be in inverse proportion to the time required for a bit line precharge operation. In other words, as the time required for the bit line precharge operation is lengthened, the magnitude of the peak current

may be decreased, but the entire programming time may be lengthened. As the time required for the bit line precharge operation is shortened, the length of the entire programming time may be shortened, but the magnitude of the peak current may be increased.

5 **[00197]** FIG. 12 is a diagram illustrating a bit line precharge operation according to an embodiment.

[00198] Referring to FIGS. 9 and 12, during a bit line precharge operation, a plurality of page buffer control signals PBSENSE1 to PBSENSE4 respectively corresponding to a plurality of page buffer groups
10 PBG1 to PBG4 may be applied to the page buffer groups PBG1 to PBG4.

[00199] A first page buffer control signal PBSENSE1, which is activated to the level of a control voltage VPB during a period from a time point tb1 to a time point tb5, may be applied to the first page buffer group PBG1. A time point at which the first page buffer control signal
15 PBSENSE1 is activated may be the time point tb1. The first page buffer group PBG1 may perform a first bit line precharge operation during a period tp1. An initiation time point of the first bit line precharge operation may be the time point tb1.

[00200] A second page buffer control signal PBSENSE2, which is
20 activated to the level of the control voltage VPB during a period from a time point tb2 to the time point tb5, may be applied to the second page buffer group PBG2. A time point at which the second page buffer control signal PBSENSE2 is activated may be the time point tb2. The second page buffer group PBG2 may perform a second bit line precharge

operation during a period $tp2$. An initiation time point of the second bit line precharge operation may be the time point $tb2$.

[00201] A third page buffer control signal $PBSENSE3$, which is activated to the level of the control voltage VPB during a period from a time point $tb3$ to the time point $tb5$, may be applied to the third page buffer group $PBG3$. A time point at which the third page buffer control signal $PBSENSE3$ is activated may be the time point $tb3$. The third page buffer group $PBG3$ may perform a third bit line precharge operation during a period $tp3$. An initiation time point of the third bit line precharge operation may be the time point $tb3$.

[00202] A fourth page buffer control signal $PBSENSE4$, which is activated to the level of the control voltage VPB during a period from a time point $tb4$ to the time point $tb5$, may be applied to the fourth page buffer group $PBG4$. A time point at which the fourth page buffer control signal $PBSENSE4$ is activated may be the time point $tb4$. The fourth page buffer group $PBG4$ may perform a fourth bit line precharge operation during a period $tp4$. An initiation time point of the fourth bit line precharge operation may be the time point $tb4$.

[00203] The length of the shortest period $tp4$, among the plurality of periods $tp1$ to $tp4$, may be fixed at a default value t_{ref} . The default value t_{ref} may be the minimum time required to precharge the potential of the bit line to a set level. The plurality of periods $tp3$, $tp2$, and $tp1$ may be sequentially increased from the shortest period $tp4$ by t_{gap} .

[00204] “ t_{gap} ” may be the interval between the initiation time points

of respective bit line precharge operations. Alternatively, "tgap" may be the interval between time points at which respective page buffer control signals are activated.

[00205] In an embodiment, during an initial period of the bit line precharge operation in which the potential of each bit line rapidly increases, power consumption may be high, and during the latter period of the bit line precharge operation in which the potential of the bit line gently increases, power consumption may be low.

[00206] In the case of FIG. 10, the page buffer control signal PBSENSE, which is activated to the level of the control voltage VPB during the period from the time point t1 to the time point t3, may be applied to all of the plurality of page buffer groups All PBG. All of the page buffer groups All PBG may simultaneously initiate the bit line precharge operations. In this case, since initial periods of bit line precharge operations of all of the page buffer groups All PBG, which has high power consumption, overlap each other, power consumption may rapidly increase, and thus a peak current exceeding a threshold value may be generated.

[00207] Apart from the embodiments of FIG. 10, FIG. 12 shows that respective page buffer groups PBG1 to PBG4 may initiate bit line precharge operations at different time points. The generation of a peak current may be prevented by prohibiting the initial periods of the bit line precharge operations, which have high power consumption between respective bit line precharge operations, from overlapping each other.

[00208] In FIG. 12, the period from the time point tb1 to the time point tb4 may correspond to the period from the time point t1 to the time point t2 of FIG. 10. The period from the time point tb4 to the time point tb5 may correspond to the period from the time point t2 to the time point t3 of FIG. 10. Therefore, in comparison with the embodiments of FIG. 10, there is an advantage in that, even if the time required for the bit line precharge operation is identical to that of FIG. 10, the generation of a peak current may be prevented.

[00209] In the case of FIG. 11, during the period from the time point ta1 to the time point ta2, a ramp signal-type page buffer control signal PBSENSE having a constant slope may be applied to all of the plurality of page buffer groups All PBG. In the case of FIG. 11, a separate ramp circuit may be required in a memory device to generate the ramp signal-type page buffer control signal PBSENSE.

[00210] In the case of FIG. 12, since square wave-type page buffer control signals PBSENSE1 to PBSENSE4 are applied to the plurality of page buffer groups PBG1 to PBG4, the potentials of the bit lines may be more rapidly increased than that of FIG. 11 for the same time. Therefore, in comparison with the embodiments of FIG. 11, there is an advantage in that the time required for the bit line precharge operation is shortened while the generation of a peak current is prevented.

[00211] In the case of FIG. 12, the square wave-type page buffer control signal may be generated using only a simpler and smaller transistor switch than the ramp circuit, and thus a layout area of the

memory device may be improved.

[00212] FIG. 13 is a diagram illustrating an operation of adjusting an interval between initiation time points of the bit line precharge operations of FIG. 12.

5 **[00213]** Referring to FIG. 13, the interval between the initiation time points of the bit line precharge operations may be adjusted from t_{gap} to $t_{gap} + \Delta t_g$. Δ may have a positive value or a negative value. In FIG. 13, a description will be made on the assumption that Δ has a positive value.

[00214] A first page buffer control signal PSENSE1, which is
10 activated to the level of a control voltage VPB during a period from a time point t_{c1} to a time point t_{c5} , may be applied to a first page buffer group PBG1. The time point at which the first page buffer control signal PSENSE1 is activated may be the time point t_{c1} . The first page buffer group PBG1 may perform a first bit line precharge operation during a
15 period $t_{p1'}$. An initiation time point of the first bit line precharge operation may be the time point t_{c1} .

[00215] A second page buffer control signal PSENSE2, which is
activated to the level of the control voltage VPB during a period from a time point t_{c2} to the time point t_{c5} , may be applied to the second page
20 buffer group PBG2. The time point at which the second page buffer control signal PSENSE2 is activated may be the time point t_{c2} . The second page buffer group PBG2 may perform a second bit line precharge operation during a period $t_{p2'}$. An initiation time point of the second bit line precharge operation may be the time point t_{c2} .

[00216] A third page buffer control signal PBOSENSE3, which is activated to the level of the control voltage VPB during a period from a time point tc3 to the time point tc5, may be applied to the third page buffer group PBG3. The time point at which the third page buffer control
5 signal PBOSENSE3 is activated may be the time point tc3. The third page buffer group PBG3 may perform a third bit line precharge operation during a period tp3'. An initiation time point of the third bit line precharge operation may be the time point tc3.

[00217] A fourth page buffer control signal PBOSENSE4, which is
10 activated to the level of the control voltage VPB during a period from a time point tc4 to the time point tc5, may be applied to the fourth page buffer group PBG4. A time point at which the fourth page buffer control signal PBOSENSE4 is activated may be the time point tc4. The fourth page buffer group PBG4 may perform a fourth bit line precharge operation
15 during a period tp4'. An initiation time point of the fourth bit line precharge operation may be the time point tc4.

[00218] The length of the shortest period tp4', among the plurality of periods tp1' to tp4', may be fixed at a default value tref. The default value tref may be the minimum time required to precharge the potential
20 of the bit line to a set level. The plurality of periods tp3', tp2', and tp1' may be sequentially increased from the shortest period tp4' by tgap+Δtg.

[00219] Referring to FIG. 7, as bit line loading is larger, the time required for the bit line precharge operation may be lengthened, whereas as bit line loading is smaller, the time required for the bit line precharge

operation may be shortened.

[00220] Therefore, it may be efficient to variably set the time required for the bit line precharge operation in consideration of bit line loading rather than uniformly setting the time required for the bit line precharge operation during the entire program operation period. The time required for the bit line precharge operation in the period having small bit line loading may be set to a time shorter than that in the period having large bit line loading, thereby shortening the entire program operation time.

[00221] In an embodiment, the interval between the initiation time points of bit line precharge operations may be adjusted depending on bit line loading. For example, the interval between the initiation time points of bit line precharge operations may be adjusted depending on the progress of the program operation. Bit line loading may be predicted based on the progress of the program operation.

[00222] When the interval between the initiation time points of the bit line precharge operations is adjusted, the lengths of periods of the bit line precharge operations may also be adjusted.

[00223] For example, when the interval between the initiation time points of bit line precharge operations is adjusted from t_{gap} to $t_{gap} + \Delta t_g$, the lengths of periods of the bit line precharge operations may be respectively adjusted from $tp1$ through $tp4$ to $tp1'$ through $tp4'$.

[00224] When the progress of the program operation has reached the time point t_a , described above with reference to FIG. 7, the interval

between the initiation time points of the bit line precharge operations may increase. That is, the value of Δ may increase. When the value of Δ increases, the lengths of periods of the bit line precharge operations respectively performed by the plurality of page buffer groups may also increase.

[00225] When the progress of the program operation has reached the time point t_b , described above with reference to FIG. 7, the interval between the initiation time points of the bit line precharge operations may decrease. That is, the value of Δ may decrease. When the value of Δ decreases, the lengths of periods of the bit line precharge operations respectively performed by the plurality of page buffer groups may also decrease.

[00226] FIG. 14 is a flowchart illustrating a program operation according to an embodiment.

[00227] Referring to FIG. 14, at step S1401, an interval (time gap) between initiation time points of bit line precharge operations may be determined based on the progress of a program operation.

[00228] The progress of the program operation may indicate a point up to which programming has been performed in the entire period of the program operation. The progress of the program operation may be a program loop count, as described above with reference to FIG. 4, or may be a highest program state, among states for which or a program verify operation has passed, as described above with reference to FIG. 5.

[00229] The interval between the initiation time points of bit line

precharge operations, respectively performed by a plurality of page buffer groups, described above with reference to FIG. 9, may be adjusted depending on the progress of the program operation, as described above with reference to FIG. 13.

5 **[00230]** At step S1403, a program operation including a program voltage apply operation and a program verify operation may be performed on a plurality of memory cells. During the program voltage apply operation, the bit line precharge operation of precharging a plurality of bit line groups coupled to the plurality of memory cells may be performed.

10 The bit line precharge operations respectively performed by the plurality of page buffer groups may be performed based on the determined interval between the initiation time points.

[00231] At step S1405, whether the program operation has been completed may be determined. When it is determined that the program
15 operation has been completed, the process is terminated, whereas when it is determined that the program operation has not been completed, the process returns to step S1401.

[00232] For example, when the plurality of memory cells have passed the program verify operation for all of states to be programmed, it may
20 be determined that the program operation has been completed. When the plurality of memory cells have failed in the program verify operation for at least one of states to be programmed, it may be determined that the program operation has not been completed.

[00233] FIG. 15 is a flowchart illustrating the program operation of

FIG. 14 according to an embodiment.

[00234] Referring to FIG. 15, at step S1501, a program loop count may be set to '0'.

[00235] At step S1503, whether the program loop count is identical
5 to a reference value may be determined. The reference value may include one or more reference values. When the program loop count is equal to the reference value, the process proceeds to step S1505, whereas when the program loop count is different from the reference value, the process proceeds to step S1507. When the process proceeds
10 to step S1505, a previous reference value may be changed to a next reference value, among the one or more reference values.

[00236] At step S1505, the interval between the initiation time points of bit line precharge operations may be adjusted. At step S1503, the progress of the program operation may be determined based on the
15 results of a comparison between the program loop count and the reference values. As described above with reference to FIG. 13, the interval between the initiation time points of the bit line precharge operations respectively performed by a plurality of page buffer groups may be adjusted depending on the progress of the program operation.

[00237] At step S1507, as the program loop progresses, the program
20 loop count may increase. Each program loop may include a program voltage apply operation and a program verify operation. During the program voltage apply operation, the bit line precharge operation may be performed. The bit line precharge operations respectively performed by

the plurality of page buffer groups may be performed based on the adjusted interval between the initiation time points.

[00238] At step S1509, whether the program operation has been completed may be determined. When it is determined that the program operation has been completed, the process is terminated, whereas when
5 it is determined that the program operation has not been completed, the process returns to step S1503. Determination about whether the program operation has been completed may be performed in a way similar to that of step S1405. However, when the program loop count
10 exceeds the preset maximum number of times, the program operation may be processed as a failure, and the process may be terminated.

[00239] FIG. 16 is a flowchart illustrating the program operation of FIG. 14 according to an embodiment.

[00240] Referring to FIG. 16, at step S1601, n may be set to '1'.

[00241] At step S1603, whether a verify-passed program state is
15 identical to a reference state may be determined. The reference state may include one or more reference states. When the verify-passed program state is identical to the reference state, the process proceeds to step S1605, whereas when the verify-passed program state is different
20 from the reference state, the process proceeds to step S1607. When the process proceeds to step S1605, a previous reference state may be changed to a next reference state, among the one or more reference states.

[00242] At step S1605, the interval between the initiation time points

of bit line precharge operations may be adjusted. At step S1603, the progress of the program operation may be determined based on the results of a comparison between the verify-passed program state and the reference states. As described above with reference to FIG. 13, the interval between the initiation time points of the bit line precharge operations respectively performed by a plurality of page buffer groups may be adjusted depending on the progress of the program operation.

[00243] At step S1607, a program pulse apply operation may be performed on a plurality of memory cells to be programmed to a program state corresponding to any one of first to k-th states (where k is a natural number of 1 or more). During the program pulse apply operation, the bit line precharge operation may be performed. The bit line precharge operations respectively performed by the plurality of page buffer groups may be performed based on the adjusted interval between the initiation time points.

[00244] At step S1609, a program verify operation for an n-th state may be performed.

[00245] For example, the program verify operation may be performed on memory cells to be programmed to the n-th state, among the first to k-th states. When all of the memory cells to be programmed to the n-th state are read as off-cells using a verify voltage corresponding to the n-th state, the memory cells may pass the program verify operation for the n-th state. When at least one of the memory cells to be programmed to the n-th state is read as an on-cell using the verify

voltage corresponding to the n-th state, the memory cells may fail in the program verify operation for the n-th state.

[00246] At step S1611, whether the program verify operation, performed at step S1609, has passed may be determined. When it is
5 determined that the program verify operation has passed, the process proceeds to step S1613, whereas when it is determined that the program verify operation has failed, the process returns to step S1607.

[00247] At step S1613, whether the program operation has been completed may be determined. When it is determined that the program
10 operation has been completed, the process is terminated, whereas when it is determined that the program operation has not been completed, the process returns to step S1615.

[00248] When all of the program verify operations for the first to k-th states have passed, it may be determined that the program operation has
15 been completed. When the program verify operation for at least one of the first to k-th states has failed, it may be determined that the program operation has not been completed.

[00249] At step S1615, n may be increased by '1'.

[00250] In accordance with the present disclosure, there are
20 provided a memory device having improved bit line precharge performance and a method of operating the memory device.

WHAT IS CLAIMED IS:

1. A memory device, comprising:

a page including a plurality of memory cells coupled to a word line;

a plurality of page buffers coupled to the plurality of memory cells

5 through a plurality of bit lines, respectively and divided into a plurality of page buffer groups each including at least two page buffers among the plurality of page buffers; and

a program operation controller configured to control the plurality of page buffers to perform bit line precharge operations initiated at different
10 time points for each page buffer group among the plurality of page buffer groups during a program operation on the page,

wherein the program operation controller increases intervals between the time points at which the bit line precharge operations are initiated by the plurality of page buffer groups at a first timing during the
15 program operation and decreases the intervals between the time points at which the bit line precharge operations are initiated by the plurality of page buffer groups at a second timing during the program operation.

2. The memory device according to claim 1, wherein:

20 the program operation controller provides a plurality of page buffer control signals that are activated at different time points to each of the plurality of page buffer groups, and

the plurality of page buffer groups perform the bit line precharge operations in response to the plurality of page buffer control signals,

respectively.

3. The memory device according to claim 2, further comprising a peripheral circuit configured to perform the program operation,

5 wherein the peripheral circuit comprises the plurality of page buffer groups, and performs a program voltage apply operation on the plurality of memory cells to be programmed to any one of first to n-th program states and a program verify operation for at least one of the first to n-th program states, where n is a natural number.

10 4. The memory device according to claim 3, wherein:
the program operation controller determines the first timing and the second timing depending on a progress of the program operation.

15 5. The memory device according to claim 4, wherein the progress of the program operation corresponds to a highest program state for which the program verify operation has passed, among the first to n-th program states.

20 6. The memory device according to claim 5, wherein the program operation controller adjusts the intervals based on a result of a comparison between the highest program state and one or more reference states.

7. The memory device according to claim 6, wherein the first timing

corresponds to a time when the highest program state is equal to or higher than a first reference state, among the one or more reference states.

8. The memory device according to claim 7, wherein the second
5 timing corresponds to a time when the highest program state is equal to or higher than a second reference state different from the first reference state, among the one or more reference states.

9. The memory device according to claim 4, wherein:
10 the peripheral circuit performs one or more program loops, each including the program voltage apply operation and the program verify operation, and

the progress of the program operation is determined based on a program loop count indicating a number of program loops that are
15 performed during the program operation.

10. The memory device according to claim 9, wherein the program operation controller adjusts the intervals based on a result of a comparison between the program loop count and one or more reference values.

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11. The memory device according to claim 10, wherein the first timing corresponds to a time when the program loop count is equal to or greater than a first reference value, among the one or more reference values.

12. The memory device according to claim 11, wherein the second timing corresponds to a time when the program loop count is equal to or greater than a second reference value different from the first reference value, among the one or more reference values.

13. The memory device according to claim 12, wherein the second reference value is greater than the first reference value.

14. The memory device according to claim 1, wherein a length of a shortest period, among periods during which the bit line precharge operations are performed, is fixed at a default value, and wherein, the default value is a minimum time required to precharge a potential of a bit line to a set value.

15. A method of operating a memory device, the memory device performing a program operation on a plurality of memory cells coupled to a plurality of page buffers through a plurality of bit lines respectively which are divided into a plurality of page buffer groups, the method comprising:

determining intervals between time points at which precharging of the plurality of bit lines is initiated by the plurality of page buffer groups; performing bit line precharge operations to precharge the plurality of bit lines coupled to the plurality of memory cells initiated at different time points for each page buffer group among the plurality of page buffer

groups; and

performing program voltage applying operations to apply a program voltage to a word line coupled to the plurality of memory cells after the bit line precharge operations,

5 wherein the intervals are increased at a first timing in the program operation and decreased at a second timing in the program operation, and

wherein each of the page buffer groups includes at least two page buffers among the plurality of page buffers.

10 16. The method according to claim 15, wherein the program operation comprises one or more program loops, and

each of the one or more program loops comprises the program voltage applying operation on the plurality of memory cells to be programmed to any one of first to n-th program states and a program verify
15 operation for at least one of the first to n-th program states, where n is a natural number.

17. The method according to claim 16, wherein the first timing and second timing are determined depending on a progress of the program
20 operation.

18. The method according to claim 17, wherein the progress of the program operation corresponds to a highest program state for which the program verify operation has passed, among the first to n-th program

states, where n is a natural number.

19. The method according to claim 18, wherein the intervals are increased or decreased based on a result of a comparison between the
5 highest program state and one or more reference states.

20. The method according to claim 17, wherein the progress of the program operation is determined based on a program loop count indicating a number of program loops that are performed during the program
10 operation.

21. The method according to claim 18, wherein the intervals are increased or decreased based on a result of a comparison between the program loop count and one or more reference values.
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22. The method according to claim 15, wherein a length of a shortest period, among periods during which the bit line precharge operations are performed, is fixed at a default value.