Description

Background of the Invention

This invention relates to the field of error prevention in microprocessor-related circuits and, more particularly, to an error prevention device which controls the microprocessor power supply as well as resetting the microprocessor.

Many so-called "deadman" timer circuits are known in the field of electronics equipment. Generally, they operate on a clock or reset signal which must be received at regular intervals. If the clock or reset signal is not received at the appropriate time, the deadman timer either switches in an alternate piece of equipment or activates some form of failure indicator. In the case of a device which includes a microprocessor, neither of these responses is satisfactory, especially since "failure" is generally not an equipment failure as such, but rather a failure mode in the microprocessor operation. Such a failure mode could be caused by noise or other spurious signal causing the microprocessor to follow the wrong instruction, provide a wrong output signal or to get caught in a loop of the program. It would be desirable to reset the microprocessor to reinitiate the program when such an error has occurred.

In US Patent 4,203,153, a battery powered microprocessor is utilized with a battery saver circuit. The microprocessor is de-energized after completion task performance and a timer is started. After a predetermined period of time, the timer causes the microprocessor to be energized to permit performance of another programmed task.

In US Patent 4,072,852, a monitoring and restarting circuit for a digital computer is disclosed. The restart circuit includes a detector circuit for detecting an in-operative state of the digital computer by monitoring periodic output signals to detect missing of a predetermined number of computer output signals. The detector circuit then produces an output signal to start a time period measuring circuit and to energize a restart signal generating means. The restart signal is applied to the digital computer to restart its operation.

The problem of resetting a microprocessor in the event of a program failure mode becomes more difficult in the environment of the present invention. Here the microprocessor is contained in a battery powered device where, in order to conserve power, the microprocessor is operated in two modes: a first high drain, fully operational mode; and a second reduced drain, reduced operational capability mode. To further minimize power drain, the microprocessor's power source also has two operational modes that correspond to the two power demand modes of the microprocessor, it is necessary to switch the power source to the full output mode as well as to reset the microprocessor. It is also a requirement that such a deadman timer circuit operate in the reduced operational capability mode of the microprocessor.

Accordingly, the invention provides a deadman timer circuit comprising input means for receiving signal pulses from a microprocessor indicative that the microprocessor is functioning properly, timing means coupled to the input means for determining if the signal pulses have been interrupted, and first output means coupled to the timing means for providing a reset pulse to the microprocessor in response to an interruption in the signal pulses for reinitializing the operation of the microprocessor; and characterized in that the circuit further comprises second output means coupled to the timing means for switching a multi-level power supply to a high output mode in response to said interruption in signal pulses thereby insuring that the multi-level power supply can provide the power required to reinitialize the microprocessor.

Brief Description of the Drawings

Fig. 1 is a block diagram illustrating the use of the invention in a paging receiver or other communication receiver.

Fig. 2 is a block diagram illustrating the circuit of the invention.

Fig. 3 is a schematic diagram of the circuit of the invention.

Detailed Description of the Preferred Embodiment

The present invention has particular application to a miniature electronic device, such as a personal pager, operating with a small battery cell and including a microprocessor for decoding communication signals. Fig. 1 shows a functional diagram of such a paging receiver utilizing the present invention. Specifically, a communications receiver 10 is connected to a selective signalling decoder 12 that comprises a microprocessor 14 and a read-only memory 16. The decoder 12 is further interconnected with an annunciation transducer 18, a DC/DC converter 20, a code memory 22 and a deadman timer 24.

The receiver 10, the DC/DC converter 20, and the deadman timer 24 are directly connected to a battery 26, which powers the operation of these blocks and is the energy souce for the DC/DC converter 20. Converter 20 generates the power supply levels needed to operate the decoder 12 which includes microprocessor 14 and the code memory 22.

In operation, the communications receiver 10 recovers signals transmitted over some communications channel and supplies that signal to the decoder 12 containing microprocessor 14. The decoder 12 in turn functions to decode the recovered signal by determining if it contains any of the one or more address signal patterns stored in code memory 22. If a pattern match is detected, the decoder 12 activates the annunciation transducer 18 and causes an appropriate alert signal to be generated to inform the user that a paging signal has been received.

In order to minimize the drain from battery 26, the decoder 12 is operated in two modes, a high power drain, fully operational mode in which it

can decode signals in real time, and a reduced power drain, reduced operational capability mode in which the decoder times the interval to the next transition to the high power drain mode. To take full advantage of the power saving, dual mode operation of the decoder, the DC/DC converter power source 20 also has two operational modes that correspond to the two modes of the decoder. That is, the converter 20 has a high output mode in which it can supply the power required to operate the decoder in its high drain, fully operational mode, and a reduced output mode in which it can supply the power required to operate the decoder in its low drain, reduced operational capability mode.

Thus, in its low output mode, the DC/DC converter is adjusted to supply a greatly diminished output power level with maximum efficiency. And, as a result, the converter cannot support the fully operational high drain mode of the decoder.

During the normal operation of the system, the microprocessor 14 controls the operation of the DC/DC converter 20 and switches the output mode of the converter in accordance with its power demands. A control output from the deadman timer 24 is also connected to the converter 20, and this signal path will place the converter 20 in the high output mode if the microprocessor should experience a program execution failure and require reinitialization.

The present invention is shown in more detail in Fig. 2, where a terminal 30 is an input terminal which couples a timed pulse signal from a selective signal decoder (not shown) into a buffer circuit 31. These signals will be two-level waveforms (as shown) comprising very brief pulses. The cessation of these pulses will indicate that something has disrupted the normal operation of the microprocessor. The output of buffer 31 is separately connected through an amplifier 32 to a first timer 34 and through an inverter 33 to a second timer 36. The received pulses are therefore separately coupled to the timing circuits 34 and 36. Timer 34 therefore detects a first error state of the microprocessor operation. Timer 34 includes means for detecting a missing pulse and, since the pulse duration is very short, amplifier 32 precedes the timer 34 to raise the level of the signals as will be further explained hereinbelow. Timer 36 includes means for detecting that the input at terminal 30 has been high for too long a period, by utilizing the output of inverter 33 which is coupled between buffer 31 and timer 36. Timer 36 serves to detect a pulse that does not end at the correct time, thus indicating that the microprocessor "failed" during a timer reset pulse. Timer 36 therefore detects a second error state of the microprocessor operation. The outputs of first timer 34 are connected to the first inputs of a NOR gate 40 and to a NOR gate 42. The outputs of second timer 36 are connected to the second input of NOR 40 and to the second input of NOR 42.

The output of NOR 40 is coupled via a terminal 44 to the mode control input of a DC/DC converter (not shown) which supplies current to the device at either a "standby" or a "fully-powered" level. Detection of either of the error states just described will cause the DC/DC converter 20 to switch to the full current output mode. The output of NOR 42 is coupled via a terminal 46 to reset and initialize the microprocessor, causing the microprocessor to go back to the starting point of the program, regardless of where the error occurs in the program.

A preferred embodiment of the circuit for the present invention is shown in Fig. 3. The buffer 31 inverts the incoming pulses supplied from the microprocessor at terminal 30 and provides separate buffered outputs to inverter 33 and amplifier 32 which includes transistors 50 and 52. A current source comprised of a transistor 54 and a resistor 56 supplies current to charge capacitors 58 and 60 in the timers 34 and 36 respectively. With the capacitor 58 discharged, a transistor 62 in the timer 34 will be non-conducting and a transistor 64 will be conducting. The capacitor 58 will begin to charge linearly and continue until the leading edge of a pulse is received at the terminal 30, causing the discharge of the capacitor. However, if a pulse should not be received, indicating an operational problem in the microprocessor, the capacitor 58 will continue charging until the transistor 62 begins to conduct. At this point transistor 62 in conductance cuts off the transistor 64 and sends a signal from the collector of the transistor 64 to each of the NOR gates 40 and 42 shown in electrical schematic form. NOR 42 is shown in two portions on either side of timer 36. The signal is supplied specifically to transistors 70 and 68 respectively.

As described before, an output signal from the NOR 40 ensures that the microprocessor is fully powered by the DC to DC converter 20 in its high power mode and an output signal from the NOR 42 resets the microprocessor, reinitializing the program. A transistor 66, also coupled to the collector of transistor 64, provides a feedback signal which discharges the capacitor 58 and turns off the transistor 62, resetting the timer 34. Since the discharge of the capacitor 58 is enabled only by the brief input pulse, the buffer amplifier 32 boosts the level of the pulse to ensure proper operation. The process of charging and discharging the capacitor 58 will then continue until another input pulse is again missed for some reason.

In timer 36, the operation is essentially as in the timer 34. The input, however, is reversed, and capacitor 60 is charged during pulses and discharged between pulses. In other words, the capacitor charges on a high level signal and discharges at a low signal. Thus, if the microprocessor program operation should fail or false during a timed pulse from the microprocessor to the deadman timer, capacitor 60 would continue charging. A transistor 72 in the timer 36 will begin to conduct, a transistor 74 will be turned off, sending a signal to transistors 76, 78 and 80 of the NOR gates 42 and 40, respectively. A transistor

80, also coupled to the collector of the transistor 74, discharges the capacitor 60 and turns off the transistor 72. The charging and discharging cycle of capacitor 60 will then continue as before in the timer 36 as long as the input pulses at the input terminal 30 continue normally.

Thus, there has been shown and described a dual deadman timer which operates to reinitialize a microprocessor in the event of a software failure in the microprocessor, and also ensures that the microprocessor is fully powered for reinitialization.

Claims

1. A deadman timer circuit comprising input means (30) for receiving signal pulses from a microprocessor (14) indicative that the microprocessor (14) is functioning properly, timing means (34, 36) coupled to the input means for determining if the signal pulses have been interrupted, and first output means (42) coupled to the timing means for providing a reset pulse to the microprocessor in response to an interruption in the signal pulses for reinitializing the operation of the microprocessor; and characterized in that the circuit further comprises second output means (40) coupled to the timing means (33, 34) for switching a multi-level power supply (20) to a high output mode in response to said interruption in signal pulses thereby insuring that the multi-level power supply can provide the power required to reinitialize the microprocessor.

2. A circuit according to claim 1 wherein the power supply has two output levels.

3. A circuit according to claim 1 or 2 wherein the power supply is a DC/DC converter.

4. A circuit according to any preceding claim wherein the timing means includes a first timer (34) responsive to a first logic level of said signal pulses and a second timer (36) responsive to a second logic level of said logic pulses, the timing means providing the reset pulse to the microprocessor and switching the multi-level power supply to the high output mode when the time duration of the first or the second logic levels exceed predetermined time intervals.

Patentansprüche

1. Totmann-Zeitgeberschaltung, enthaltend eine Eingabeeinrichtung (30) zum Aufnehmen von Sugnalimpulsen von einem Mikroprozessor (14), die anzeigen, daß der Mikroprozessor (14) ordnungsgemäß arbeitet, eine Zeitgebereinrichtung (34, 36), die mit der Eingabeeinrichtung verbunden ist, um zu ermitteln, ob Signalimpulse unterbrochen worden sind, und eine erste Ausgabeeinrichtung (42), die mit der Zeitgebereinrichtung verbunden ist, um dem Mikroprozessor einen Rücksetzimpuls in Abhängigkeit von einer Unterbrechung der Signalimpulse zuzuführen, um den Betrieb des Mikroprozessors wieder zu initialisieren; und dadurch gekennzeichnet, daß die Schaltung weiterhin eine zweite Ausgabeeinrichtung (40) enthält, die mit der Zeitgebereinrichtung (33, 34) verbunden ist, um eine Mehrpegelstromversorgung (20) auf einen hohen Ausgangsmode in Abhängigkeit von der Unterbrechung der Signalimpulse zu schalten, um dadurch sicherzustellen, daß die Mehrpegelstromversorgung die für die Wiederinitialisierung des Mikroprozessors erforderliche Leistung zur Verfügung stellen kann.

2. Schaltung nach Anspruch 1, bei der die Stromquelle zwei Ausgangspegel hat.

3. Schaltung nach Anspruch 1 oder 2, bei der die Stromquelle ein Gleichspannungs/Gleichspannungs-Wandler ist.

4. Schaltung nach einem der vorhergehenden Ansprüche, bei der die Zeitgebereinrichtung einen ersten Zeitgeber (34) enthält, der auf einen ersten Logikpegel der Signalimpulse anspricht, und einen zweiten Zeitgeber (36) enthält, der auf einen zweiten Logikpegel der Logikimpulse anspricht, wobei die Zeitgebereinrichtung den Rücksetzimpuls an den Mikroprozessor abgibt und die Mehrpegelstromversorgung auf den hohen Ausgangsmodus schaltet, wenn die Zeitdauer der ersten und zweiten Logikpegel vorbestimmte Zeitintervalle überschreiten.

Revendications

1. Circuit horloge d'ancrage comprenant un moyen d'entrée (30) pour recevoir des impulsions de signal d'un microprocesseur (14) indiquant que le microprocesseur (14) fonctionne correctement, un moyen de synchronisation (34, 36) couplé au moyen d'entrée pour déterminer si les impulsions de signal ont été interrompues, et un premier moyen de sortie (42) couplé au moyen de synchronisation pour fournir une impulsion de remise à l'état initial au microprocesseur en réponse à une interruption dans les impulsions de signal pour réinitialiser le fonctionnement du microprocesseur; et caractérisé en ce que le circuit comprend en outre un second moyen de sortie (40) couplé au moyen de synchronisation (33, 34) pour commuter une source d'alimentation à plusieurs niveaux (20) dans un mode de sortie élevée en réponse à ladite interruption des impulsions de signal pour garantir ainsi que la source d'alimentation à plusieurs niveaux peut fournir la tension d'alimentation nécessaire pour réinitialiser le microprocesseur.

2. Circuit selon la revendication 1, dans lequel la source d'alimentation a deux niveaux de sortie.

3. Circuit selon l'une quelconque des revendications 1 et 2, dans lequel la source d'alimentation est un convertisseur de courant continu CC/CC.

4. Circuit selon l'une quelconque des revendications 1 à 3, dans lequel le moyen de synchronisation comprend une première horloge (34) réagissant à un premier niveau logique des impulsions de signal et une seconde horloge (36) réagissant à un second niveau logique des impulsions logiques, le moyen de synchronisation fournissant l'impulsion de remise à l'état initial au

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* C L M S *

microprocesseur et commutant la source d'alimentation à plusieurs niveaux dans le mode de sortie élevée quand la durée du premier ou du second niveau logique dépasse des intervalles de temps prédéterminés.

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