

ABSTRACT

A memory device includes a memory cell array including normal memory cells and redundant memory cells; first page buffers connected to the normal memory cells through first bit lines including a first bit line group and a second bit line group and arranged in a first area corresponding to the first bit lines in a line in a first direction; and second page buffers connected to the redundant memory cells through second bit lines including a third bit line group and a fourth bit line group and arranged in a second area corresponding to the second bit lines in a line in the first direction, wherein, when at least one normal memory cell connected to the first bit line group is determined as a defective cell, normal memory cells connected to the first bit line group are replaced with redundant memory cells connected to the third bit line group.

FIG. 8