CLAIMS

1. A clock circuit, comprising:

at least two first driving circuits and a plurality of discrete first wires located between adjacent first driving circuits, wherein the adjacent first driving circuits are connected through at least one first wire and at least two second wires, the first driving circuits are connected with the second wires, all of the first wires connected between two second wires are connected in series with each other, the first wires are located on a first metal layer, the second wires are located on a second metal layer, and the second metal layer is above the first metal layer;

second driving circuits, wherein adjacent second driving circuits are connected through third wires, a resistance between the adjacent second driving circuits is equal to a resistance between the adjacent first driving circuits, a total length of the third wires between the adjacent second driving circuits is larger than a total length of the first wires between the adjacent first driving circuits, and a resistance per unit length of the third wires is smaller than a resistance per unit length of the first wires.

2. The clock circuit of claim 1, wherein the first wires extend in a first direction, lengths of different first wires are equal in the first direction, the plurality of first wires are arranged side by side in a second direction, and the first direction is perpendicular to the second direction.

3. The clock circuit of claim 1, wherein the first wires are U-shaped, the plurality of first wires are arranged side by side in a second direction, and orthographic projections of the different second wires in the second direction coincide.

4. The clock circuit of claim 1, wherein a resistance per unit length of the second wires is smaller than the resistance per unit length of the first wires, and a metal layer where the third wires are located is above the first metal layer.

5. The clock circuit of claim 1, wherein the resistance per unit length of the third wires is smaller than or equal to a resistance per unit length of the second wires.

6. The clock circuit of claim 5, wherein a metal layer where the third wires are located is above the second metal layer, or the third wires are located on the second metal layer.

7. The clock circuit of claim 1, further comprising:

a first function module, comprising at least two first driving circuits, and configured to receive a first signal and generate and output a second signal based on the first signal, wherein the second signal serves as an internal feedback signal of the clock circuit; and

a second function module, comprising at least two second driving circuits, and configured to receive a third signal and generate and output a fourth signal based on the third signal, wherein the first signal and the third signal are clock signals with the same phase, and the output end of the second function module serves as the output end of the clock circuit.

8. The clock circuit of claim 7, wherein the first function module comprises a first function unit and a second function unit which are sequentially connected, and the second function module comprises a third function unit and a fourth function unit which are sequentially connected, wherein the first function unit is configured to receive the first signal, the second functional unit is configured to output the second signal, the third function unit is configured to receive the third signal, the fourth function unit is configured to output the fourth signal, a number of the first driving circuits contained in the first function unit is equal to a number of the second driving circuits contained in the third function unit, and a number of the first driving circuits contained in the second function unit is equal to a number of the second driving circuits contained in the fourth functional unit.

9. The clock circuit of claim 8, wherein the first function unit and the third function unit are clock trees, the second function unit and the fourth function unit are signal drivers, the first signal and the third signal are clock signals for data transmission, and the second signal and the fourth signal are clock signals for data readout.

10. The clock circuit of claim 1, wherein the first driving circuits comprise inverters.

11. The clock circuit of claim 1, wherein the first wires and the second wires are electrically connected through at least one conductive via.

12. A memory, comprising the clock circuit of any of claims 1-11.

13. A method for manufacturing a semiconductor structure, comprising:

calculating a number of second driving circuits according to a preset delay duration,

and after determining the number of the second driving circuits, calculating a length of a connection between adjacent second driving circuits according to a length of a preset conductive path, wherein the adjacent second driving circuits are connected through third wires;

providing at least two first driving circuits and providing a plurality of discrete first wires located between adjacent first driving circuits, wherein a number of the first driving circuits is the same as a number of the second driving circuits, the first wires are located on a first metal layer, and a metal layer where the third wires are located is above the first metal layer;

calculating a number of the first wires, designated as an initial number, connected in series between the first driving circuits according to the length of the connection, a resistance per unit length of the third wires, a resistance per unit length of the first wires and a length of each first wire, so that an ideal value of resistance between the adjacent first driving circuits is equal to an ideal value of resistance between the adjacent second driving circuits; and

providing second wires, so that the initial number of the first wires are connected in series between the adjacent first driving circuits, the second wires are connected with the first driving circuits, all of the first wires connected between two second wires are connected in series with each other, the second wires are located on the second metal layer, and the second metal layer is above first metal layer.

14. The method for manufacturing a semiconductor structure of claim 13, further comprising: after providing the second wires,

simulating a first resistance between adjacent first driving circuits and a second resistance between adjacent second driving circuits to obtain an actual value of the first resistance and an actual value of the second resistance; and

if the actual value of the first resistance is not equal to the actual value of the second resistance, adjusting a layout of the second wires connected in series between the adjacent first driving circuits according to a difference between the actual value of the first resistance and the actual value of the second resistance so as to adjust the number of the first wires connected in series between the adjacent first driving circuits, wherein an adjusted ideal value of the first resistance is equal to the actual value of the second resistance.

15. The method for manufacturing a semiconductor structure of claim 14, wherein adjusting the layout of the second wires connected in series between the adjacent first driving circuits comprises: adjusting positions of the second wires and positions of conductive vias, so that the second wires are connected to another first wire through the conductive vias.