

Bipolar Transistor with Raised Extrinsic Base fabricated in an Integrated BiCMOS Circuit

TECHNICAL FIELD

The present invention relates generally to bipolar transistors and, more particularly, to a process for forming a bipolar transistor with a raised extrinsic base in an integrated bipolar and complementary metal-oxide-semiconductor (BiCMOS) transistor circuit.

BACKGROUND OF THE INVENTION

Transistors are used as either amplifying or switching devices in electronic circuits. In the first application, the transistor functions to amplify small ac signals. In the second application, a small current is used to switch the transistor between an “on” state and an “off” state.

The bipolar transistor is an electronic device with two p-n junctions in close proximity. The bipolar transistor has three device regions: an emitter, a collector, and a base disposed between the emitter and the collector. Ideally, the two p-n junctions (the emitter-base and collector-base junctions) are in a single layer of semiconductor material separated by a specific distance. Modulation of the current flow in one p-n junction by changing the bias of the nearby junction is called “bipolar-transistor action.”

External leads can be attached to each of the three regions and external voltages and currents can be applied to the device using these leads. If the emitter and collector are doped n-type and the base is doped p-type, the device is an “nnp” transistor. Alternatively, if the opposite doping configuration is used, the device is a “pnp” transistor. Because the mobility of minority carriers (i.e., electrons) in the base region of npn transistors is higher than that of holes in the base of pnp transistors, higher-frequency operation and higher-speed performances can be

obtained with npn devices. Therefore, npn transistors comprise the majority of bipolar transistors used to build integrated circuits.

As the vertical dimensions of the bipolar transistor are scaled more and more, serious device operational limitations have been encountered. One actively
5 studied approach to overcome these limitations is to build transistors with emitter materials whose band gaps are larger than the band gaps of the material used in the base. Such structures are called heterojunction transistors.

Heterostructures comprising heterojunctions can be used for both majority carrier and minority carrier devices. Among majority carrier devices,
10 heterojunction bipolar transistors (HBTs) in which the emitter is formed of silicon (Si) and the base of a silicon-germanium (SiGe) alloy have recently been developed. The silicon-germanium alloy (often expressed simply as silicon-germanium) is narrower in band gap than silicon.

The advanced silicon-germanium bipolar and complementary
15 metal-oxide-semiconductor (BiCMOS) technology uses a silicon-germanium base in the heterojunction bipolar transistor. In the high frequency (such as multi-GHz) regime, conventional compound semiconductors such as GaAs and InP currently dominate the market for high speed wired and wireless communications. Silicon-germanium BiCMOS promises not only a comparable performance to GaAs
20 in devices such as power amplifiers, but also a substantial cost reduction due to the integration of heterojunction bipolar transistors with standard CMOS, yielding the so-called "system on a chip."

For high performance HBT fabrication, yielding SiGe/Si HBTs, a conventional way to reduce the base resistance is through ion implantation onto the extrinsic base.
25 The ion implantation will cause damage, however, to the base region. Such damage ultimately may lead to degradation in device performance.

To avoid the implantation damage, a raised extrinsic base (REXT) is formed by depositing an extra layer of polycrystalline silicon (or silicon-germanium) atop the

conventional SiGe extrinsic base layer. There are essentially two processes that may be applied to achieve such a raised extrinsic base. The first process involves selective epitaxy; the other involves chemical-mechanical polishing (CMP).

1. Selective Epitaxy

5 In a typical selective epitaxy process, the raised extrinsic base polycrystalline silicon is formed before the deposition of the intrinsic base SiGe. The intrinsic base SiGe is deposited selectively onto the exposed surface of silicon and polycrystalline silicon inside an over-hanging cavity structure. The selective epitaxy with a cavity structure mandates stringent process requirements for good selectivity,
10 and suffers from poor process control.

US-A-5 523 606 discloses a process using selective epitaxy. Referring to Figs. 1A and 1B, which correspond to portions of Figures 7C and 7E, respectively, of the '606 patent, the extrinsic base poly silicon 21 is deposited before the intrinsic base 23 is deposited. Shown in Fig. 1A are silicon nitride film 15, silicon nitride side
15 wall spacers 17, and semiconductor substrate 1. The films (not labeled) underneath the extrinsic base poly silicon 21 are etched away to form a cavity (or void) 22 of an over-hanging structure. The intrinsic base 23 is then selectively deposited, as shown in Fig. 1B, only inside the cavity 22 on the silicon and polysilicon exposed surface. See '606 patent from column 8, line 53 to column 9, line 17. Fig. 1B also
20 shows an n-type epitaxial collector layer 13. The approach disclosed in the '606 patent avoids a CMP step, but has several drawbacks such as poor process control in filling the cavity 22 and stringent requirements for selective deposition conditions.

US-A-5 620 908 applies an approach similar to that disclosed in the
25 '606 patent. Specifically, as illustrated in Figure 6F of the '908 patent and discussed in column 13 (specifically, at lines 24-26), there is disclosed a process that incorporates selective epitaxy and the step of etching an overhang to form a cavity.

2. CMP

The second type of process that can be applied to form a raised extrinsic base involves a CMP step. US-A-5 015 594 proposes the formation of extrinsic base polysilicon by CMP. The isolation is achieved by thermal oxidation, however, which is not feasible in high performance devices due to the high temperature thermal process.

Y.C. Sun and J. Warnock disclose a process, in "Process for a High-Performance Bipolar-Based BICMOS," IBM Technical Disclosure Bulletin, vol. 35, no. 4B, pages 295-97 (Sept. 1992), of forming a raised extrinsic base by CMP. The extrinsic base portion is formed in direct contact with the intrinsic base, however, without any etch stop. Figs. 2A and 2B correspond to Figure 1 of the article. With reference to Figs. 2A and 2B, the extrinsic base polysilicon 21 is deposited directly above the intrinsic base region 5, which is also on the emitter opening region, without any interfacial films to stop the emitter opening etch 31 of the extrinsic base polysilicon 21. This process exhibits poor process control and, therefore, cannot yield good production control and cannot yield a highly reliable and reproducible bipolar device.

To stop the extrinsic polysilicon etch during formation of the emitter opening, an etch stop layer of dielectric materials such as oxide must be disposed underneath the extrinsic base polysilicon. This etch stop layer cannot cover the whole extrinsic base region, however, in order to form an electrical contact between the raised extrinsic base and the underneath base 25. Therefore, a need remains for a feasible approach to achieve those required features with CMOS circuit integration capability.

The deficiencies of the conventional methods show that a need still exists for an improved process of fabricating an HBT with a raised extrinsic base. To overcome the shortcomings of the conventional methods, a new process is provided. An object of the present invention is to form an HBT with a raised extrinsic base by CMP integrated in a CMOS circuit. A related object is to properly design

the thickness of the emitter sacrificial plug and the CMOS gate stack so that the two structures have the same height across the entire wafer, with a flat top surface, to serve as a polish-stop layer for the formation of the raised extrinsic base as well as the isolation dielectric layer by CMP.

- 5 Another related object is to provide a fabrication process including a specific layer sequence and predetermined range of layer thicknesses for the HBT with a raised extrinsic base formed by CMP integrated in a CMOS circuit. Still another object of the present invention is to provide a process in which the CMOS gate dielectric stack is designed to form a flat surface aligned with the HBT emitter plug. Finally, a
- 10 general object of the present invention is to provide a process sequence to form an entire BiCMOS circuit incorporating CMP process steps.

SUMMARY OF THE INVENTION

To achieve these and other objects, and in view of its purposes, the present invention provides a process for forming a bipolar transistor with a raised

15 extrinsic base, an emitter, and a collector integrated with a complementary metal-oxide-semiconductor (CMOS) circuit with a gate. An intermediate semiconductor structure is provided having a CMOS area and a bipolar area. An intrinsic base layer is provided in the bipolar area. A base oxide is formed across, and a sacrificial emitter stack of silicon layer (referred to below as an emitter stack

20 silicon layer) is deposited on, both the CMOS and bipolar areas. A photoresist is applied to protect the bipolar area and the structure is etched to remove the emitter stack silicon layer from the CMOS area only such that the top surface of the emitter stack silicon layer on the bipolar area is substantially flush with the top surface of the CMOS area. Finally, a polish stop layer is deposited having a substantially flat top

25 surface across both the CMOS and bipolar areas suitable for subsequent chemical-mechanical polishing (CMP).

Two specific embodiments of the present invention are possible, depending upon the relative thicknesses of the various layers. In the first embodiment, the thickness of the emitter stack silicon layer is approximately equal

to the thickness of the silicon gate of the CMOS area. The process then uses the base oxide as an etch stop such that the top surface of the emitter stack silicon layer on the bipolar area is substantially flush with the top surface of the base oxide in the CMOS area.

5 In the second embodiment, the thickness of the emitter stack silicon layer plus the thickness of the intrinsic base layer is approximately equal to the thickness of the silicon gate of the CMOS area. The process then includes the step of etching to remove both the emitter stack silicon layer, the base oxide, and the intrinsic base layer from the CMOS area only, with a CMOS protective layer acting
10 as an etch stop. This step assures that the top surface of the emitter stack silicon layer on the bipolar area is substantially flush with the top surface of the protective layer in the CMOS area.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, but are not restrictive, of the
15 invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is best understood from the following detailed description when read in connection with the accompanying drawing. It is emphasized that, according to common practice, the various features of the
20 drawings are not to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. Included in the drawings are the following figures:

Figs. 1A and 1B correspond to a portion of Figures 7C and 7E, respectively, of US-A- 5 523 606;

25 Figs. 2A and 2B correspond to Figure 1 of above mentioned article by Y.C. Sun and J. Warnock, "Process for a High-Performance Bipolar-Based

BICMOS," IBM Technical Disclosure Bulletin, vol. 35, no. 4B, pages 295-97 (Sept. 1992);

Fig. 3 shows the structure that results following application of the first three steps of the process of the present invention;

5 Fig. 4 illustrates the fourth step of the process of the present invention, highlighting several types of areas having different topographies;

Fig. 5 illustrates the fifth step of the process of the present invention, highlighting the clear difference in the topography (a step) between the CMOS area and the bipolar area;

10 Fig. 6 highlights the different topography between the bipolar and CMOS areas after deposition of the emitter stack silicon and SiN polish stop layers, rendering it impractical to planarize the bipolar area to form the raised extrinsic base with a good polish stop;

15 Fig. 7 illustrates a first embodiment of the process according to the present invention, which renders the surface of the a-Si on the bipolar area flush with the top surface of the base oxide in the CMOS area;

Fig. 8 illustrates a second embodiment of the process according to the present invention, which renders the surface of the a-Si on the bipolar area flush with the top surface of the TEOS layer atop the gate polysilicon in the CMOS area;

20 Fig. 9 illustrates the structure of Fig. 8 after a silicon nitride layer is deposited as the polish stop layer;

Fig. 10 illustrates the next step of the process according to either embodiment of the present invention, showing formation of an extrinsic base opening through the emitter stack of SiN and a-Si;

Fig. 11 illustrates formation of a spacer;

Fig. 12 illustrates removal of the base oxide in the extrinsic base opening and formation of the raised extrinsic base;

Fig. 13 illustrates formation of a planar isolation layer;

5 Fig. 14 shows the structure resulting after the planar isolation layer is stripped from the CMOS area;

Fig. 15 shows the structure resulting after etching, using the planar isolation layer as a mask, the stack of the silicon nitride layer and the a-Si layer in the emitter island and in the supporting island;

10 Fig. 16 shows the structure resulting after an emitter polysilicon layer is deposited, a SiN layer is deposited as a mask to form the emitter contact, and a photoresist is coated on the structure;

Fig. 17 shows the structure resulting after the SiN layer and the emitter polysilicon layer are removed outside the emitter area, using the photoresist as a
15 mask, and a photoresist layer corresponding to the extrinsic base region and covering the CMOS region is applied; and

Fig. 18 shows the structure resulting after all of the oxide layers are stripped, a SiN etch stop is deposited, a borophosphosilicate glass layer is deposited and planarized, and the various contacts for the emitter, base, collector,
20 and other components are formed to complete the integration of the structure.

DETAILED DESCRIPTION OF THE INVENTION

CMP has been extensively used to form the shallow trench isolation (STI) and the back-end-of-line (BEOL) isolation regions during semiconductor fabrication. Conventional processes have not addressed, however, using CMP to
25 achieve planarization for silicon devices fabricated in a BiCMOS circuit with different

topography between the bipolar and CMOS areas. The formation of the STI uses a dielectric layer as the polish stop, which is deposited directly onto the flat surface of a silicon substrate in the early stage of the wafer processing.

In the process of the present invention, the extrinsic base layer is deposited over an emitter sacrificial plug. The extrinsic base can be polycrystalline silicon, or "PC" silicon, which is often referred to as "polysilicon." The thicknesses of the sacrificial plug and the rest of the CMOS area are properly adjusted so as to achieve a pre-polish flat surface for planarization by CMP. The major differences between the process of the present invention and conventional methods of forming the raised extrinsic base by CMP for an HBT integrated in a CMOS circuit are (a) the extrinsic base layer in the present invention is deposited over an emitter sacrificial plug, and (b) the sacrificial plug and the rest of the CMOS areas have their thicknesses properly adjusted to achieve a pre-polish flat surface for CMP planarization. The detailed steps of the process according to the present invention, for fabricating the bipolar device with a raised extrinsic base by CMP integrated into a CMOS circuit, are provided below.

Referring now to the drawing, in which like reference numbers refer to like elements throughout, Fig. 3 shows the result of the first three steps of the process of the present invention. The starting structure includes a silicon active area 100 with a dielectric-filled isolation region 110 and a buried collector region 105. A protective layer 120 is deposited and opened for CMOS fabrication. The protective layer 120 protects the bipolar area. Although the bipolar area is an NPN-type in the example described, the bipolar area is not limited to that type. This completes the first step of the process.

In a second step, conventional CMOS devices (including a PFET 140 and an NFET 150) are fabricated, with p-well and n-well implantation followed by appropriate threshold voltage adjustment doping. The gate dielectric is formed, then the gate conductor 130 is deposited. In a third step, a protective dielectric layer 160 is deposited to provide CMOS protection. An optional layer 170 may be deposited

to facilitate nucleation of the subsequent base. These first three steps yield the structure illustrated in Fig. 3.

These steps are followed by opening up a bipolar region using conventional photolithography and by etching the protective layers 170, 160, and 5 120, as shown in Fig. 4. Fig. 4 also shows the STI area 108 and the base opening 180.

As shown in Fig. 5, the epitaxial SiGe base 190 is deposited using techniques well known to those skilled in the art. A thin layer (typically less than 50 nm) of a dielectric such as an oxide may be formed for passivation. The deposition 10 of epitaxial SiGe base 190 and the formation of base passivation layer 200 are conventional and well known to the artisan. Fig. 5 highlights the clear difference in the topography, step 210, between the CMOS area 175 and the bipolar area 165. The step 210 is approximately equal to the height (1 002- 50 nm) of the gate conductor 130.

15 Fig. 6 highlights the different topography between the bipolar and CMOS areas. After the base oxide 200, a stack of a-Si layer 230 and a SiN layer 240 is deposited, each layer about 50-200 nm and preferably 100-150 nm in thickness. The SiN layer 240 will be used as the polish stop for the following steps. Note the height difference, step 250, by which the NPN bipolar area 165 is lower 20 than the CMOS area 175. Step 250 is about the same as the CMOS gate thickness (step 210). If the topography remains with the SiN layer 240 standing high on the CMOS area, step 250, it is impractical to planarize the bipolar area 165 to form the raised extrinsic base with a good polish stop: there is no polish stop layer with a flat surface to form the raised extrinsic base via CMP.

25 The solution resides in providing a pre-polish stop layer with a planar or flat surface across the entire wafer, taking into account the different topography between the CMOS and NPN areas as shown in Fig. 6. A pre-polish flat surface is provided by properly designing the layer sequence and the thicknesses of the deposited materials. Both the layer sequence and the thicknesses are

“predetermined” because they are reasonably predictable within a certain range, as opposed to random, and calculated to achieve a desired end product.

To resolve the identified topography issue, the films deposited before the polish stop SiN layer 240 must be flush across the wafer. A flush surface can be realized by a masked etch process. In this process, a photoresist 235 is used to protect the bipolar area 165. The CMOS area 175 is exposed and the films are etched away with a proper etch stop. The next step is deposition of the polish stop SiN layer 240. The top surface of the polish stop SiN layer 240 will be flush across both the CMOS and bipolar areas.

There are two options for this process depending on the layer thickness in the structure. The first option is illustrated in Fig. 7, in which the thickness of the a-Si 230 is approximately equal to the thickness of the gate conductor 130. After the base oxide 200 is formed, the emitter stack a-Si 230 is first deposited. The a-Si 230 thickness is chosen so as to be equal to the step height difference Δ , the same as the difference between the CMOS stack and the NPN epitaxial SiGe base 190, which is about the same as the gate conductor 130. The photoresist masked etching will stop on the base oxide 200; the a-Si 230 is removed only in the CMOS area 175 by the resist mask etch. The result is that the surface of the a-Si 230 on the bipolar area 165 is flush with the top surface of the base oxide 200 in the CMOS area 175. Therefore, the subsequently formed SiN layer 240 will have a flat top surface across the entire wafer for both the CMOS and bipolar areas.

The second option is illustrated in Fig. 8, in which the thickness of the a-Si 230 plus the thickness of the epitaxial SiGe base 190 is about equal to the thickness of the gate conductor 130. Because the thickness of the gate conductor 130 is about 200 nm, often greater than the thickness of the a-Si 230 of about 50-150 nm, it is feasible to etch the a-Si 230 further through the base oxide 200 with the underlying epitaxial SiGe base 190 also removed. The etch will stop on the CMOS protective layer 160. This process requires that the combination of the two films (a-Si 230 and the epitaxial SiGe base 190) have a thickness equal to the gate

conductor 130. Therefore, the surface of the a-Si 230 on the bipolar area 165 is flush with the top surface of the CMOS protective layer 160.

Fig. 9 illustrates the structure of Fig. 8 after SiN layer 240 is deposited. (An etch stop layer of TEOS 245, about 10-50 nm thick, is optional atop the SiN layer 240.) Note that the top surface of the SiN layer 240 on the bipolar area 165 is flush with the top surface on the CMOS area 175, necessary for the next step CMP.

Because the fabrication process is similar for both options in the following steps, the second option (Figs. 8 and 9) will be used as an example to discuss the bipolar fabrication. The process steps that would complete the fabrication for the structure of the first option (Fig. 7) can be directly derived based on the discussion below. Such steps would be known to the artisan in view of the example based on the second option.

In the next step of the process according to the present invention, the extrinsic base opening resist block is coated (not shown). As shown in Fig. 10, the stack RIE of layer 240 and the layer 230 forms an extrinsic base opening 270, leaving an emitter island 280 and a supporting island 290. The RIE step stops at the base oxide layer 200.

As illustrated in Fig. 11, a spacer 300 is formed next. The spacer 300 can be a single or a composite dielectric spacer. The base oxide 200 is stripped in the extrinsic base opening 270. The base oxide 200 on other areas is protected by the emitter island 280 and the supporting island 290.

Fig. 12 shows that a raised extrinsic base 310 is formed. Extrinsic base 310 is formed, for example, by depositing a polysilicon layer 313 and subsequently planarizing back to a level 315 that fills the extrinsic base opening 270 using layer 240 as the polish stop, followed by recess etching back. The raised extrinsic base

310 can also be formed by selective epitaxy deposition only on the exposed extrinsic base opening 270.

Fig. 13 shows that a dielectric isolation layer 323 is deposited. A CMP step is applied to the isolation layer 323 to planarize that layer, forming planar isolation layer 320. The layer 240 is again used as a polish stop in this step.

Next, a photoresist mask of the same image as photoresist 235 can be used to block the bipolar area 165. Then the remaining isolation layer 320 on the CMOS area 175 (along with any residue films from the spacers if applicable) is stripped. The resulting structure is illustrated in Fig. 14.

10 The process of the present invention next uses the planar isolation layer 320 as a mask. The sacrificial stack layers 230 and 240 in the emitter island 280 and in the supporting island 290 are etched away. The etch stops at the protective layer 160 in the CMOS area 175 and at the base oxide 200 in the bipolar area 165. The resulting structure is illustrated in Fig. 15.

15 As shown in Fig. 16, the base oxide layer 200 is etched within the emitter opening and an emitter layer 350 is deposited. Then a dielectric protective layer 360 is deposited as a mask to form the emitter contact. A photoresist 370 is provided to facilitate subsequent processing.

Using the photoresist 370 as a mask, the dielectric protective layer 360 and the emitter layer 350 are removed outside the emitter area. The planar isolation layer 320 and the CMOS protective layer 160 serve as etch stops. A photoresist layer 380, patterned to cover both the extrinsic base region and the CMOS region 175, is applied as illustrated in Fig. 17 and opened. A directional etch is applied to the exposed regions, first etching oxide isolation layer 320 and base oxide layer 200, then the polysilicon films of raised extrinsic base 310 and NPN epitaxial SiGe base 190, stopping on the protective layer 160. The dielectric protective layer 160 is then

removed through wet or dry etch techniques and (optionally) CMOS implants and anneals may take place.

All of the following steps, of forming the contacts to the emitter, base, and collector of the bipolar area 165 and the contacts to the source, drain, and gate
5 of the CMOS area 175, are well-known to the artisan. A SiN etch stop 430 is deposited, followed by deposition and planarization of a borophosphosilicate glass (BPSG) layer 440. The formation of various contacts 450 for the emitter, base, collector, and other components completes the integration of the structure. Such structure is illustrated in Fig. 18.

10 A number of important differences should now be apparent between the fabrication process of the present invention and the conventional methods. Several major differences exist between the present invention and the disclosure in the article by Y.C. Sun and J. Warnock. Among those differences are: (a) the extrinsic base polysilicon in the present invention is deposited over an emitter
15 sacrificial plug, and (b) the sacrificial plug and the rest of the CMOS areas have their thicknesses properly adjusted to provide a pre-polish flat surface to achieve the CMP planarization. In the referenced article, in contrast, the polish stop is assumed to be the CMOS gate dielectric. In the present invention, the CMOS top surface is no longer the same height as the emitter plug by default, and to achieve this flat
20 surface is one of the important objects of the present invention.

Several major differences also exist between the present invention and the disclosure of USA- 5 523 606. Two of those differences are highlighted. First, the extrinsic base polysilicon of the present invention is deposited after the intrinsic base formation. Second, the extrinsic base is formed via CMP made possible by
25 proper film stack design to provide a polish stop, and hence no selective epitaxy is necessary for the intrinsic SiGe base.

CLAIMS

1. A process for forming a bipolar transistor with a raised extrinsic base, an emitter, and a collector integrated with a complementary metal-oxide-semiconductor (CMOS) circuit, the process comprising the steps of:

5 (a) providing an intermediate semiconductor structure having a bipolar area and a CMOS area with a gate conductor;

(b) providing an intrinsic base layer, having a thickness, in the bipolar area;

(c) forming a base oxide across both the CMOS and bipolar areas;

10 (d) depositing on both the CMOS and bipolar areas an emitter stack silicon layer having a thickness;

(e) applying a photoresist to protect the bipolar area;

(f) etching to remove the emitter stack silicon layer from the CMOS area only such that the top surface of the emitter stack silicon layer on the bipolar
15 area is substantially flush with the top surface of the CMOS area; and

(g) depositing a polish stop layer having a substantially flat top surface across both the CMOS and bipolar areas suitable for subsequent chemical-mechanical polishing (CMP).

2. The process according to claim 1, wherein the thickness of the
20 emitter stack silicon layer deposited in step (d) is approximately equal to the thickness of the gate conductor of the CMOS area and the process further comprises, in step (f), using the base oxide as an etch stop such that the top surface of the emitter stack silicon layer on the bipolar area is substantially flush with the top surface of the base oxide in the CMOS area.

3. The process according to claim 1, wherein the thickness of the emitter stack silicon layer deposited in step (d) plus the thickness of the intrinsic base layer provided in step (b) is approximately equal to the thickness of the gate conductor of the CMOS area and the process further comprises, in step (f), etching
5 to remove both the emitter stack silicon layer and the base oxide from the CMOS area only, with a CMOS protective layer acting as an etch stop, such that the top surface of the emitter stack silicon layer on the bipolar area is substantially flush with the top surface of the protective layer in the CMOS area.

4. The process according to claim 1, wherein the polish stop layer
10 is a dielectric.

5. The process according to claim 1, wherein the bipolar transistor is a heterojunction bipolar transistor and the intrinsic base layer is silicon-germanium.

6. The process according to claim 1, wherein the emitter stack
15 silicon layer comprises:

(a) an a-Si layer having a thickness of 50-2 00 nm; and

(b) a SiN polish stop layer having a thickness of 50-2 00 nm.

7. The process according to claim 2, wherein the gate conductor has a thickness of 1 00-2 50 nm and the emitter stack silicon layer comprises:

20 (a) an a-Si layer having a thickness of 50-2 00 nm; and

(b) a SiN polish stop layer having a thickness of 50-2 00 nm.

8. The process according to claim 3, wherein the gate conductor has a thickness of 1 00-2 50 nm and the emitter stack silicon layer comprises:

(a) an a-Si layer having a thickness of 50-2 00 nm; and

(b) a SiN polish stop layer having a thickness of 50-2 00 nm..

9. The process according to claim 1, further comprising the step (h) of etching to form an extrinsic base opening, the etch stopping at the base oxide.

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10. The process according to claim 9, further comprising the steps of (i) forming a spacer, and (j) stripping the base oxide from the extrinsic base opening.

11. The process according to claim 10, further comprising the step
10 of (k) forming the raised extrinsic base in the extrinsic base opening.

12. The process according to claim 11, further comprising the steps of (l) depositing an isolation layer, and (m) using the flush surface of the polish stop layer to apply CMP to form a planar isolation layer.

13. The process according to claim 12, further comprising the steps
15 of (n) applying a photoresist to protect the bipolar area, and (o) stripping the planar isolation layer from the CMOS area.

14. The process according to claim 13, further comprising the step of (p) using the planar isolation layer as a mask and etching the emitter stack silicon layer and the polish stop layer, the etch stopping at the base oxide in the bipolar
20 area and at a CMOS protective layer in the CMOS area.

15. The process according to claim 14, further comprising the steps of (q) depositing an emitter stack silicon layer, and (r) depositing a mask to form the emitter contact.

16. The process according to claim 15, further comprising the step (s) of forming an extrinsic base pattern by simultaneously covering with photoresist the extrinsic base and the CMOS area then etching.

17. The process according to claim 16, further comprising the step (t) of forming the various contacts for the emitter, base, and collector of the bipolar area and the various contacts for the source, drain, and gate of the CMOS area.

18. An intermediate semiconductor structure useful during the process of forming a bipolar transistor with a raised extrinsic base, an emitter, and a collector integrated with a complementary metal-oxide-semiconductor (CMOS) circuit, the structure comprising:

a bipolar area;

a CMOS area including a top surface, a gate conductor having a thickness, and a protective layer with a top surface;

an intrinsic base layer, having a thickness, in the bipolar area;

15 a base oxide across both the CMOS and bipolar areas, the base oxide having a thickness;

an emitter stack silicon layer only on the bipolar area and over the base oxide, the emitter stack silicon layer having a thickness and a top surface substantially flush with the top surface of the CMOS area; and

20 a polish stop layer having a substantially flat top surface across both the CMOS and bipolar areas suitable for subsequent chemical-mechanical polishing (CMP).

19. The intermediate semiconductor structure according to claim 18, wherein the thickness of the emitter stack silicon layer is approximately equal to the thickness of the gate conductor of the CMOS area and the top surface of the emitter

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stack silicon layer on the bipolar area is substantially flush with the top surface of the base oxide in the CMOS area.

20. The intermediate semiconductor structure according to claim 18, wherein the thickness of the emitter stack silicon layer plus the thickness of the
5 intrinsic base layer is approximately equal to the thickness of the gate conductor of the CMOS area and the top surface of the emitter stack silicon layer on the bipolar area is substantially flush with the top surface of the protective layer in the CMOS area.

21. The intermediate semiconductor structure according to claim 18,
10 wherein the polish stop layer is a dielectric.

22. The intermediate semiconductor structure according to claim 18, wherein the bipolar transistor is a heterojunction bipolar transistor and the intrinsic base layer is silicon-germanium.

23. The intermediate semiconductor structure according to claim 18,
15 wherein the emitter stack silicon layer comprises:

(a) an a-Si layer having a thickness of 50-2 00 nm; and

(b) a SiN polish stop layer having a thickness of 50-2 00 nm.

24. The intermediate semiconductor structure according to claim 19, wherein the gate conductor has a thickness of 1 00-2 50 nm and the emitter stack
20 silicon layer comprises:

(a) an a-Si layer having a thickness of 50-2 00 nm; and

(b) a SiN polish stop layer having a thickness of 50-2 00 nm.

25. The intermediate semiconductor structure according to claim 20, wherein the gate conductor has a thickness of 1 00-2 50 nm and the emitter stack silicon layer comprises:

(a) an a-Si layer having a thickness of 50-2 00 nm; and

5 (b) a SiN polish stop layer having a thickness of 50-2 00 nm.