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SEMICONDUCTOR DEVICE ASSEMBLIES AND PACKAGES INCLUDING MULTIPLE SEMICONDUCTOR DEVICES AND METHODS

TECHNICAL FIELD

The present invention relates generally to stacked semiconductor device assemblies and packages, as well as to associated assembly and packaging methods. More particularly, the invention pertains to multidie assemblies and packages with low profiles and minimal size.

BACKGROUND

The dimensions of many different types of state of the art electronic devices are ever decreasing. To reduce the dimensions of electronic devices, the structures by which the microprocessors, memory devices, other semiconductor devices, and other electronic components of these devices are packaged and assembled with carriers, such as circuit boards, must become more compact. In general, the goal is to economically produce a chip-scale package (CSP) of the smallest size possible, and with conductive structures, such as leads, pins, or conductive bumps, which do not significantly contribute to the overall size in the X, Y, or Z dimensions, all while maintaining a very high performance level.

One approach to reducing the sizes of assemblies of semiconductor devices and circuit boards has been to minimize the profiles of the semiconductor devices and other electronic components upon carrier substrates (e.g., circuit boards) so as to reduce the distances the semiconductor devices protrude from the carrier substrates. Various types of packaging technologies have been developed to facilitate orientation of semiconductor devices upon carrier substrates in this manner.

Conventionally, semiconductor device packages have been multilayered structures, typically including a bottom layer of encapsulant material, a carrier (e.g., leads, a circuit board, etc.), a semiconductor die, and a top layer of encapsulant material, for example. In addition, the leads, conductive bumps, or pins of conventional semiconductor device packages, which electrically connect such packages to carrier substrates, as well as provide support for the packages, are sometimes configured to space the semiconductor device packages apart from a carrier substrate.

As a result, the overall thicknesses of these semiconductor device packages and the distances the packages protrude from carrier substrates are greater than is often desired for use in state of the art electronic devices.

"Flip-chip" technology, as originating with controlled collapse chip connection (C-4) technology, is an example of an assembly and packaging technology that results in a semiconductor device being oriented substantially parallel to a carrier substrate, such as a circuit board. In flip-chip technology, the bond pads or contact pads of a semiconductor device are arranged in an array over a major surface of the semiconductor device. Flip-chip techniques are applicable to both bare and packaged semiconductor devices. A packaged flip-chip type semiconductor device, which typically has solder balls arranged in a so-called "ball grid array" (BGA) connection pattern, typically includes a semiconductor die and a carrier substrate, which is typically termed an "interposer". The interposer may be positioned adjacent either the back side of the semiconductor die or the active (front) surface thereof.

When the interposer is positioned adjacent the back side of the semiconductor die, the bond pads of the semiconductor die are typically electrically connected by way of wire bonds or other intermediate conductive elements to corresponding contact areas on a top side of the interposer. These contact areas communicate with corresponding bumped contact pads on the back side of the interposer. This type of flip-chip assembly is positioned adjacent a higher-level carrier substrate with the back side of the interposer facing the carrier substrate.

If the interposer is positioned adjacent the active surface of the semiconductor die, the bond pads of the semiconductor die may be electrically connected to corresponding contact areas on an opposite, top surface of the interposer by way of intermediate conductive elements that extend through one or more holes formed in the interposer. Again, the contact areas communicate with corresponding contact pads on the interposer. In this type of flip-chip semiconductor device assembly, however, the contact pads are also typically located on the top surface of the interposer. Accordingly, this type of flip-chip assembly is positioned adjacent a higher-level carrier substrate, such as a printed circuit board, by orienting the interposer with the top surface facing the carrier substrate.

In each of the foregoing types of flip-chip semiconductor devices, the contact pads of the interposer are disposed in an array that has a footprint that mirrors an arrangement of corresponding terminals or other contact regions formed on a carrier substrate. Each of the bond (on bare flip-chip semiconductor dice) or contact (on flip-chip packages) pads and its corresponding terminal may be electrically connected to one another by way of a conductive structure, such as a solder ball, that also spaces the interposer some distance away from the carrier substrate.

The space between the interposer and the carrier substrate may be left open or filled with a so-called "underfill" dielectric material that provides additional electrical insulation between the semiconductor device and the carrier substrate. In addition, each of the foregoing types of flip-chip semiconductor devices may include an encapsulant material covering portions or substantially all of the interposer and/or the semiconductor die.

The thicknesses of conventional flip-chip type packages having ball grid array connection patterns are defined by the combined thicknesses of the semiconductor die, the interposer, the adhesive material therebetween, and the conductive structures (e.g., solder balls) that protrude above the interposer or the semiconductor die. As with the flat packages, conventional flip-chip type packages are often undesirably thick for use in small, thin, state of the art electronic devices. Furthermore, use of this general construction method for producing a stacked multichip module (MCM) results in a relatively high-profile, large footprint device.

Thinner, or low-profile, flip-chip type packages have been developed which include interposers or other carriers with recesses that are configured to receive at least a portion of the profiles of semiconductor devices. While interposers that include recesses for partially receiving semiconductor devices facilitate the fabrication of thinner flip-chip type packages, the semiconductor dice of these packages, as well as intermediate conductive elements that protrude beyond the outer surfaces of either the semiconductor dice or the interposers, undesirably add to the thicknesses of these packages.

U.S. Patents 5,541,450 and 5,639,695, both issued to Jones et al. (hereinafter "the '450 and '695 Patents"), disclose another type of flip-chip type package, which includes an interposer with a semiconductor die receptacle extending completely

therethrough. The '695 Patent teaches a package that may be formed by securing a semiconductor die directly to a carrier substrate and electrically connecting the interposer to the carrier substrate before the semiconductor die is electrically connected to the interposer. The semiconductor die, intermediate conductive elements that connect bond pads of the semiconductor die to corresponding contact areas on the interposer, and regions of the interposer adjacent the receptacle may then be encapsulated. While this method results in a very low-profile flip-chip type package, the package cannot be tested separately from the carrier substrate. As a result, if the package is unreliable, it may also be necessary to discard the carrier substrate and any other components thereon. Moreover, the packaging method of the '695 Patent complicates the process of connecting semiconductor devices and other electronic components to a carrier substrate. In addition, it should be noted that in order to obtain a low-profile package, it may be necessary to sacrifice footprint compactness. The footprint area of such a low-profile package may be significantly greater than the area of the semiconductor die thereof.

Thus, there is a need for multidie assemblies and packages that have low profiles and relatively small footprints and for methods for fabricating such assemblies and packages.

DISCLOSURE OF INVENTION

The present invention comprises a semiconductor device package including an interposer and a plurality of semiconductor devices in a vertical or stacked arrangement. The invention includes various embodiments of the device package and methods for assembling and packaging two or more semiconductor devices with an interposer. The semiconductor device package may comprise a chip scale multichip package (CSMCP) which is configurable in various ways for use in a variety of applications, including as a memory package. The package may be formed with a thickness not much greater than the cumulative thicknesses of the devices and, also, may have a relatively small "footprint".

The package interposer of the present invention includes a substantially planar substrate with a receptacle formed therein and extending substantially therethrough, i.e., from the upper surface to the lower surface thereof. The receptacle is considered to be

a first level of the package and is configured to receive one or more semiconductor devices (e.g., semiconductor dice), which will be collectively referred to herein as "first-level" semiconductor devices. The receptacle may be configured to accept several devices in a side-by-side manner and/or stacked arrangement. In addition, the interposer includes conductors on both major surfaces thereof. The conductors may include circuit traces, level(s) of submerged traces, conductive vias connecting the traces, and conductive bond pads and/or contact areas for attachment of bond wires, solder balls or other intermediate conductive elements, discrete conductive elements, and outer connectors. The first-level semiconductor device(s) may be electrically attached to the interposer or to a second-level semiconductor device at least partially superimposed relative to the interposer.

A "second-level" (e.g., upper) semiconductor device is at least partially superimposed relative to the interposer and generally to the first-level semiconductor device(s) within the interposer receptacle. The second-level semiconductor device may have its active surface facing upwardly, with its bond pads electrically connected to corresponding contact areas on the upper surface of the interposer by way of somewhat laterally extending intermediate conductive elements. Alternatively, peripheral contact areas on the second-level semiconductor device may be flip-chip bonded to contact areas on the interposer. If the first-level semiconductor device is flip-chip connected to corresponding contact areas on the active surface of the second-level semiconductor device, the active surfaces of the first- and second-level semiconductor devices face each other. Conductive traces and vias extend from the conductive areas on the interposer to corresponding outer connectors on the interposer, which are arranged in an array over the lower surface of the interposer. For small footprint packages, microvias having a diameter as small as 50 microns or smaller may be used and may be directly attached to bond pads or solder ball contact areas, for example, greatly decreasing the interposer area required for connections within a package.

Optionally, a structure such as a film or tape (e.g., a pressure-sensitive, adhesive-coated film) may be positioned on the lower side of the interposer to cover the receptacle opening, thereby closing off the bottom end of the receptacle to facilitate the positioning of one or more semiconductor devices within the receptacle. The film may be removably secured to the interposer, thereby facilitating the removal of the film

following attachment of the second semiconductor device or an encapsulation process. Thus, a further reduction in the thickness of the package may be achieved.

As already indicated, more than one semiconductor device may be positioned within the receptacle. If a film covers the lower end of the receptacle, the device(s) may be secured to the film (e.g., tape or other member) to fix the position of the semiconductor device(s) relative to the substrate of the interposer. The first assembly level, which is coplanar with the interposer, may comprise several sublevels at which semiconductor devices are positioned in a generally coplanar configuration or in a stacked arrangement.

A "third-level" semiconductor device may be positioned below the lower surface of the interposer and connected thereto, such as by a ball grid array (BGA) connection pattern of electrical connectors or other known elements and arrangements for making electrical connections. Each of the semiconductor devices communicates with the outer connectors of the package through electrical conductors, such as metal traces, bond pads, contact areas, or conductive vias.

A so-called "underfill" dielectric material may be placed in the interstices between the semiconductor devices and the interposer to secure the semiconductor devices to the interposer and to provide additional electrical insulation between the semiconductor devices and the interposer. For example, a liquid underfill polymeric material may be permitted to flow into the narrow interstitial spaces within the package and substantially fill the spaces by capillary action. Thermal or other cure methods may be used. In addition, or alternatively, the multidie package may be subjected to additional (full or partial) encapsulation, for example, by transfer molding, pot molding, or injection molding techniques. Multidie packages incorporating teachings of the invention may be encapsulated with the second and/or third semiconductor devices fully enclosed or, optionally, with their back sides exposed. The latter configuration further reduces the profile dimension.

The multidie packages may be configured to be integrally stacked to form packages of greater numbers of devices. The outer connectors, e.g., a BGA, on the lower surface of an upper package are joined to an array of corresponding contact areas on the upper surface of a lower package.

The multidie packages of this invention have a low profile, whereby the overall height is not much greater than the combined heights of the plurality of devices in each package. Furthermore, this low profile is achieved while simultaneously maintaining a package footprint which is only slightly larger than the footprint of the largest device in the package. In some configurations, the package footprint is essentially identical to the footprint of the largest device.

As described herein, the first-level or lower semiconductor device is smaller (in footprint) than the second-level (or upper) semiconductor device. Where a third-level semiconductor device is placed below the interposer, it is typically intermediate in footprint size, i.e., between the sizes of the first- and second-level semiconductor devices.

Several exemplary methods for assembling the multidie packages in accordance with the invention are presented. Each of the methods includes the initial formation of (a) a first multidie wafer of semiconductor devices (first-level semiconductor devices), (b) a second multidie wafer of semiconductor devices (second-level semiconductor devices), (c) additional multidie wafers of semiconductor devices if desired to be incorporated in the package, at a third-level, for example, and (d) a multi-interposer sheet or strip of substrate (rigid or flexible), having through-receptacles formed in individual interposer portions. The order of subsequent steps of assembly depends upon the final package configuration which is to be formed. Generally, each package is fully formed on a multi-interposer sheet or strip and singulated therefrom following device attachment and encapsulation.

An exemplary method for assembling a semiconductor multidevice package (SCMDP) includes (a) singulating the first-level semiconductor devices, positioning them in the receptacles of the interposers, and wire-bonding their bond pads to contact areas on the upper surface of the interposer; (b) singulating the second-level semiconductor devices, attaching them atop the interposers with a die-attach tape or adhesive, and wire-bonding their bond pads to other contact areas on the upper surface of the interposer; (c) applying an encapsulating material to fill the interstitial spaces and, optionally, to cover outer surfaces of the interposer and devices, and (d) singulating individual packages from the substrate sheet or strip. Outer connectors may

be formed on the lower surface of the interposer (substrate) at any of several steps in the assembly process.

In another method for assembling a semiconductor device package in accordance with teachings of the present invention, (a) first-level semiconductor devices are singulated and attached, flip-chip style, to the active surface of the second-level semiconductor devices, typically with a BGA, (b) the second-level semiconductor devices, carrying the first-level semiconductor devices, are singulated and attached to the interposers in flip-chip style (active surface down), so that the first-level semiconductor devices are enclosed in the interposer receptacles, and (c) the sheet or strip of packages is encapsulated and individual packages singulated from the sheet or strip.

In a further assembly method utilizing flip-chip technology, second-level semiconductor devices are first singulated and attached in flip-chip arrangement to the sheet or strip of substrate and at least partially cover the upper ends of the receptacles. First-level semiconductor devices are then singulated and positioned within the receptacles of the inverted substrate sheet/strip. The first-level semiconductor devices are then joined to the second-level semiconductor devices in flip-chip fashion, followed by encapsulation and package singulation.

The encapsulant material may be disposed over the active surface of each semiconductor device located within the receptacle, as well as over intermediate conductive elements that connect the bond pads to their corresponding conductive areas on a surface of the interposer and adjacent portions of that surface of the interposer. Once each semiconductor device is held in place within the receptacle by encapsulant material, the tape or film (if used) that previously held the one or more semiconductor devices in place may be removed.

In the inventive packaging method, the various devices and interposer are substantially completed prior to assembly to form the multichip package. Conductive structures on each device and interposer are formed using known processes to ensure accurate continuity of the desired electrical connections between the package's devices and a carrier substrate.

The present invention also includes variations of the multichip packages of semiconductor devices, as further described.

Although various embodiments of the invention are described and illustrated herein, it is recognized that these embodiments are exemplary only and not exhaustive. Other configurations, features and advantages of the present invention will become apparent to those of ordinary skill in the art through consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF DRAWINGS

In the drawings, which illustrate exemplary embodiments for carrying out the invention:

FIG. 1 is a perspective view of an exemplary multidie semiconductor device package in accordance with teachings of the invention;

FIG. 1A is a perspective view of another exemplary multidie semiconductor device package in accordance with teachings of the invention;

FIG. 1B is a perspective view of a further exemplary multidie semiconductor device package in accordance with teachings of the invention;

FIG. 2 is a cross-sectional side view of a multidie semiconductor device package in accordance with teachings of the present invention, as taken along line 2-2 of FIG. 1;

FIG. 2A is a cross-sectional side view of another embodiment of a multidie semiconductor device package in accordance with teachings of the present invention;

FIG. 2B is a cross-sectional side view of a further embodiment of a multidie semiconductor device package in accordance with teachings of the invention;

FIG. 3 is a cross-sectional side view of another multidie semiconductor device package formed in accordance with teachings of the invention, as taken along line 2-2 of FIG. 1;

FIG. 4 is a cross-sectional side view of a further multidie semiconductor device package formed in accordance with the invention, as taken along line 2-2 of FIG. 1;

FIG. 5 is a cross-sectional side view of a stacked package of two multidie semiconductor device packages in accordance with teachings of the invention;

FIG. 6 is a cross-sectional side view of another multidie semiconductor device package formed in accordance with teachings of the invention, as taken along line 2-2 of FIG. 1;

FIG. 7 is a cross-sectional side view of yet another embodiment of a multidie semiconductor package formed in accordance with the invention, as taken along line 2-2 of FIG. 1;

FIG. 8 is a cross-sectional side view of a further embodiment of a multidie semiconductor package formed in accordance with the invention;

FIG. 9 is a cross-sectional side view of an additional embodiment of a multidie semiconductor package formed in accordance with the invention;

FIG. 10 is a cross-sectional side view of a multidie semiconductor package formed of three devices in accordance with the invention;

FIG. 11 is a cross-sectional side view of a further embodiment of a multidie semiconductor package formed of three devices in accordance with the invention;

FIG. 12 is a cross-sectional side view of a multidie semiconductor package formed of four semiconductor devices in accordance with a method of the invention;

FIGS. 13A - 13I depict a method for forming a multidie semiconductor package in accordance with teachings of the invention;

FIGS. 14A - 14I depict another method for forming a multidie semiconductor package in accordance with the invention; and

FIGS. 15A - 15K depict yet another method for forming a multidie semiconductor package in accordance with the invention.

Dimensions of elements in the figures are not necessarily to scale in order to provide clarity in understanding. Like numerals are used to identify like elements throughout the drawings and description.

BEST MODE(S) FOR CARRYING OUT THE INVENTION

Referring to FIG. 1, a multichip semiconductor device package 10 according to the present invention is illustrated. As shown, FIG. 1 is an external view of the package 10 and is representative of a large number of possible device configurations exemplified in the figures following FIG. 1. Package 10 is illustrated as having an upper surface 12, a lower surface 14, and peripheral edges 16. Outer connectors 18, shown here as solder balls in a ball grid array (BGA) connection pattern, are depicted as being on the lower surface 14 of the package 10 and attached to contact areas 9 on a representative carrier substrate 8. The dimensions of the package 10 include length 11,

width 13 and vertical thickness 15 (exclusive of the distance outer connectors 18 protrude from the lower surface 14). The outline of the encapsulated package 10, comprising length 11 and width 13 dimensions, defines the "footprint" of the package 10. The package 10 shown in FIG. 1 represents a multidie package which has been encapsulated in a mold.

FIG. 1A depicts another package configuration, in which the back side 44 of an upper semiconductor device 40 is left uncovered in the encapsulation step.

In FIG. 1B, another package configuration is shown with encapsulant 90 surrounding semiconductor device 40 and visibly extending to an interposer 61. The back side 44 of semiconductor device 40 is shown as uncovered but, of course, the encapsulation process may be operated to encase back side 44 as well.

FIG. 2 illustrates one embodiment of package 10 which depicts the upper surface 66 of interposer 61, including conductors 70, contact areas 71A and 71B, and traces 72. Also pictured is a first-level semiconductor device 20 positioned in receptacle 65 and having its bond pads 30 wirebonded by intermediate conductive elements 32 to contact areas 71A. The outline of a second-level semiconductor device 40 is also shown. The interposer 61 of package 10 is formed of a substantially planar substrate 60 having a receptacle 65 formed therein, i.e., extending from an upper surface 66 to a lower surface 68 of the substrate 60. The interposer 61 has conductors 70 on its upper surface 66 including traces 72 and contact areas 71A and/or 71B. The lower surface 68 is shown with conductors 74, including contact areas 75 to which outer connectors 18, e.g., balls, bumps, columns, pillars, or pins of conductive material (e.g., solder, another metal or metal alloy, conductive or conductor-filled elastomer, etc.), are attached. The upper surface conductors 70 and lower surface conductors 74 are depicted as being connected by conductive vias 78 in the form of microvias having a very small diameter, e.g., less than about 300 microns. Intermediate levels of conductors (not shown) may be provided within the interposer 61 and connected by conductive vias 78. The conductive vias 78 may be formed by photoimaging, laser ablation, plasma etching or the so-called "B^2IT" process, for example.

The substrate 60 of interposer 61 may be formed from either a rigid or flexible material. For example, the substrate 60 may be formed from silicon or another

semiconductive material (e.g., gallium arsenide, indium phosphide, etc.), with at least some surfaces thereof being lined with an electrically insulative material to prevent shorting of the various electrical circuits running thereacross. Alternatively, other suitable interposer substrate materials may be used to form the substrate 60, including, without limitation, FR-4 resin, BT resin, ceramic, and polyimide. The substrate 60 may have a laminated structure comprising sublayers, or plies, of one or more materials.

Receptacles 65 may be part of the originally formed substrate 60, or may be subsequently formed by "routing" or by a photo, laser or plasma technique, for example. A large number of interposers 61 may simultaneously be formed in the format of a substrate sheet or strip 62 (FIG. 14F), and all receptacles 65 therein formed sequentially or substantially simultaneously.

In this discussion, the position of each semiconductor device relative to the interposer 61 will be noted as being at a "first-level", i.e., within the receptacle 65, at a "second-level," i.e., above the upper surface 66 of the interposer 61, or at a "third-level", i.e., below the lower surface 68 of the interposer 61. In addition, sublevels may exist within each level, each sublevel being occupied by a semiconductor device. Thus, a wide range of semiconductor device combinations may be achieved to meet a particular package's electronic footprint and thickness constraints for a particular purpose, whether that is for a microprocessor, memory device, or other purpose.

As depicted in FIG. 2, a first-level semiconductor device 20, or die, is positioned within receptacle 65 and generally coplanar with the interposer 61, having its active surface 22 facing upwardly. The back side 24 of the first-level semiconductor device 20 may be approximately coplanar with the lower surface 68 of the interposer 61 and may become part of the lower surface 14 of the package 10. Bond pads 30 on the active surface 22 of first-level semiconductor device 20 are electrically connected to contact areas 71A on the interposer 61 by intermediate conductive elements 32 (e.g., bond wires, conductive tape-automated bonding (TAB) elements carried by a dielectric, polymer film, thermocompression or ultrasonically bonded leads, etc.). The bond pads 30 of first-level semiconductor device 20 may be located on the active surface 22, either along a central axis of the semiconductor device 20 peripherally or otherwise, as known in the art.

A second-level semiconductor device 40 is positioned above the interposer 61 and attached thereto by an adhesive material 58 in the form of film, tape, or a flowable polymer, for example. The spacing between the second-level semiconductor device 40 and interposer 61 is maintained to accommodate intermediate conductive elements 52, minimize electrical interference between the second-level semiconductor device 40 and one or both of the first-level semiconductor device 20 and the interposer 61 to produce a low-profile package 10. The active surface 42 of second-level semiconductor device 40 has bond pads 50 which are shown connected to contact areas 71B by intermediate conductive elements 52.

As shown in FIG. 2, the package 10 is encapsulated in an insulating encapsulant material 90 by any suitable method. The package 10 as shown is typical of encapsulation by transfer molding, a process used widely in the semiconductor industry. Alternatively, pot molding or injection molding processes may be used. The encapsulant 90 encloses the second-level semiconductor device 40, including its active surface 42 and intermediate conductive elements 52 attached to the interposer 61. The upper surface 66 of interposer 61 is also enclosed in encapsulant 90, as are interstitial spaces 80 between the semiconductor devices 20, 40 and the interposer 61.

The receptacle 65 may be formed somewhat centrally within the substrate 60 and is laterally confined by the material of the substrate 60. The receptacle 65 is configured to receive one or more first-level semiconductor devices 20 in such a manner that the active surface 22 of each semiconductor device is positioned for electrical attachment of the first-level semiconductor device 20 to the interposer 61. The receptacle 65 may be smaller in size than the second-level semiconductor device 40 in at least one dimension (length or width). Likewise, the first-level semiconductor device(s) 20 may have smaller footprints than the second-level semiconductor device(s) 40. The interstitial spaces 80 may be filled with an encapsulating material for supporting and protecting the first-level semiconductor device 20 and sealing the active surface 22 thereof.

In the embodiment of FIG. 2, interposer 61 includes contact areas 71A and 71B (e.g., contact pads) formed on the upper surface 66 thereof. Contact areas 71A are adjacent the receptacle 65 for wirebonding to bond pads 30 on the active surface(s) 22 of the first-level semiconductor device(s) 20. Each contact area 71B corresponds with

and is configured to be electrically connected, via intermediate conductive elements 52, such as the depicted bond wires, conductive TAB elements carried by dielectric polymer film, thermocompression or ultrasonically bonded leads, or the like, to bond pads 50 on the active surface 42 of the second-level semiconductor device 40. Thus, the contact areas 71B are located outside of the second-level semiconductor device 40 to facilitate electrical connection to the intermediate conductive elements 52. The conductive elements 32, 52; bond pads 30, 50; contact areas 71A, 71B, 75; traces 72; and vias 78 may comprise, for example, aluminum, gold, silver, conductive alloys, or the like.

Conductive traces 72 extend substantially laterally from each contact area 71A, 71B, on or through the interposer 61, to corresponding conductors 70 arranged in an array over the upper surface 66 of the interposer 61. Generally, each conductor 70 communicates with a conductive via 78, which passes through the interposer 61 to contact area 75 on the lower surface 68 of the interposer 61. Outer connections 18, such as solder balls, are connected to the contact areas 75, enabling ready connection to contact areas (not shown) of a carrier substrate (not shown) (e.g., a circuit board, another semiconductor device, etc.).

Some of the conductors 70 and corresponding conductive vias 78 may alternatively be positioned near the receptacle 65. As shown in FIG. 2A, a variation of the interposer 61′ includes contact areas 71A and 71B that may directly overlie conductive vias 78. Thus, in a package 10′ including interposer 61′, the first-level semiconductor device 20 is connected to outer connectors 18, which are secured to contact areas 75 located at an opposite end of each conductive via 78 and which, therefore, lie directly below contact areas 71A and 71B. Alternatively, as depicted in FIG. 2B, another embodiment 10″ of a package incorporating teachings of the present invention includes another variation of interposer 61″. Interposer 61″ includes conductive traces 76 on the lower surface 68 thereof, which may extend laterally outward from the conductive vias 78 to more peripherally located contact areas 75 to which outer connectors 18 are secured.

The outer connectors 18 are shown in the drawings as comprising solder balls or bumps. However, various conductive structures 18, such as columns, pillars, or other structures formed from a conductive material, such as solder, metal, or z-axis

conductive elastomer including one or more discrete, anisotropically conductive regions, may be secured to contact areas 75 to facilitate communication between the plurality of semiconductor devices of the semiconductor device package 10 and a carrier substrate, another package or other apparatus.

As shown in FIG. 2, package 10 also includes a quantity of dielectric encapsulant material 90 within the interstitial space 80 adjacent the interposer 61 and first-level semiconductor device 20, in the space surrounding the second-level semiconductor device 40 and overlying the interposer 61. The encapsulant material 90 at least partially secures and laterally confines each first-level semiconductor device 20 within the receptacle 65 and secures and protects the second-level semiconductor device 40 (and any additionally mounted devices). Various methods for partial or complete encapsulation of multidie semiconductor package 10 are described hereinafter.

FIG. 3 illustrates another embodiment of the multidie semiconductor device package 110. This embodiment differs from that of FIG. 2 in that the second-level semiconductor device 40 is mounted on interposer 61 in a flip-chip arrangement and is shown connected to contact areas 71B on the interposer by discrete conductive elements 56, balls, bumps, pillars, columns, or pins formed from conductive material, such as solder, conductive or conductor-filled elastomer, z-axis conductive elastomer, or the like. In other respects, this embodiment is similar to that of FIG. 2.

Configuring second-level semiconductor device 40 to be mounted in a flip-chip arrangement provides a package 110 with a reduced profile, inasmuch as intermediate conductive elements 52 are eliminated. Nevertheless, the package 110 is shown with encapsulant material 90 covering the second-level semiconductor device 40.

The package 110′ of FIG. 4 differs from the package of FIG. 3 only in that the encapsulant material 90 is mold-applied to leave the back side 44 of the second-level semiconductor device 40 uncovered. For many applications, additional covering of the back side 44 is unnecessary; eliminating this encapsulant provides a further reduction in profile (package thickness 15 in FIG. 1).

Another feature of the present invention is that two or more packages of the invention may be stacked to combine a larger number of semiconductor devices in a low-profile, small footprint manner. Shown in FIG. 5 are two packages 110, 110′

having a configuration like that of FIGS. 3 and 4, except they are only partially encapsulated to leave room for outer connectors 18A between the packages 110, 110′ and to leave outer connectors 18 exposed beneath package 110. The packages are joined in a package stack 88 by intermediate connectors 18A; e.g., solder balls of package 110′ are joined to contact areas 71 on the upper surface 66 of the interposer 61 of lower package 110. The package stack 88 may be further encapsulated to enclose intermediate outer connectors 18A and fill interstitial spaces 80A between the packages 110 and 110′. Other intermediate connectors 18A may be used in place of solder balls, including bumps, columns, etc., as known in the art.

FIG. 6 illustrates another embodiment of semiconductor device package 110″ with a very low profile (i.e., a profile that is only slightly larger than the combined thicknesses of the stacked semiconductor devices 20, 40 thereof) and very small footprint (i.e., a footprint that is about the same as or only slightly larger than that of the second-level semiconductor device 40 thereof). In this package 110″, the interposer 61″ is configured to be only slightly larger than the second-level semiconductor device 40. This package 110″ is particularly configured for use in miniature electronic apparatus of all types. The density of conducting elements in and on the interposer 61″ is shown to be generally inversely proportional to the fraction of interposer area consumed by the receptacle 65.

All of the packages discussed thus far include a first-level semiconductor device 20 which is electrically connected to an interposer by way of elongate intermediate conductive elements 32. In FIG. 7, an embodiment of package 110‴ is depicted in which the first-level semiconductor device 20 is attached in flip-chip style to the back side 44 of the second-level semiconductor device 40 by way of solder balls 36 positioned between bond pads 30 of the first-level semiconductor device 20 and corresponding bond pads 59 on back side 44 of the second-level semiconductor device 40. Conductive traces 84 that are carried on the back side 44 of the second-level semiconductor device 40 extend from bond pads 59 toward an outer periphery of the second-level semiconductor device 40. Discrete conductive elements 82 electrically connect conductive traces 84 on the back side 44 of the second-level semiconductor device 40 to corresponding conductive traces 72 on the interposer 61. The second-level semiconductor device 40 is, in turn, electrically connected by elongate intermediate

conductive elements 52 to contact areas 71B on the upper surface 66 of the interposer 61.

FIGS. 8, 9, 10, 11 and 12 depict variations of package 10 in which the semiconductor devices are all connected in flip-chip fashion, either to the interposer 61 or to each other.

In the package 210 of FIG. 8, bond pads 30 on the active surface 22 of a first-level semiconductor device 20′ are attached to contact areas 59 on the active surface 42 of a second-level semiconductor device 40 by discrete conductive elements 36A, shown comprising conductive balls, although bumps, pillars, columns, regions of films, and other structures formed from metal, conductive or conductor-filled elastomer, or the like (e.g., an anisotrophic or z-axis-conductive film) could also be used. Conductive traces 54 on the active surface 42 of the second-level semiconductor device 40 connect the contact areas 59, via discrete conductive elements 56, traces 72, conductors 70 and conductive vias 78, to contact areas 75 and outer connectors 18. Bond pads 50 on the second-level semiconductor device 40 electrically communicate in a like manner with outer connectors 18. Although the first-level semiconductor device 20′ in this example is shown with two centrally arranged rows of discrete conductive elements 36A, a semiconductor device 20′ with peripherally located discrete conductive elements 36A may be used with a second-level semiconductor device 40 that has shorter conductive traces 54 extending over the active surface 42 thereof.

FIG. 9 depicts a package 210′ which varies from the embodiments already described. In the package 210′ of FIG. 9, a first-level semiconductor device 20 is not mounted within the interposer receptacle 65. Instead, a third-level semiconductor device 100 is mounted with an active surface 102 thereof facing upward toward the receptacle 65 and the lower surface 68 of the interposer 61 and secured to the lower surface 68 with adhesive material 117. Bond pads 118 on the third-level semiconductor device 100 are shown connected to the active surface 42 of the second-level semiconductor device 40 by discrete conductive elements 116. The back side 104 of third-level semiconductor device 100 is shown uncovered, but may be encapsulated. In FIG. 9, the interposer 61 is shown as being formed from a flexible or so-called "flex" substrate material of a known type, which typically has a reduced thickness relative to rigid substrates.

FIG. 10 shows a multidie package 210'' which combines features of the packages 210, 210' of FIGS. 8 and 9, respectively. A first-level semiconductor device 20 is positioned within receptacle 65 and attached, flip-chip style, to a second-level semiconductor device 40 positioned above the interposer 61. The bond pads of semiconductor device 20 and, thus, the discrete conductive elements 36 may be arranged either peripherally, as shown, or centrally on first-level semiconductor device 20. The second-level semiconductor device 40 is attached in a flip-chip manner to the upper surface 66 of the interposer 61, whereby discrete conductive elements 56 communicate signals from both the first-level and second-level semiconductor devices 20, 40 to the interposer 61 and, thence, to outer connectors 18.

A third-level semiconductor device 100' is attached, flip-chip style, to the lower surface 68 of interposer 61. Peripherally located bond pads 118 on semiconductor device 100' are connected to contact areas 75 of the interposer 61 by discrete conductive elements 116 such as balls, bumps, pillars, or columns of conductive material, such as metal or conductive or conductor-filled elastomer, or electrically distinct regions of an anisotrophically or z-axis conductive film. Conductive traces 76 between contact areas 75 and outer connectors 18 complete the package circuit. It should be noted that the size of outer connectors 18 is selected so that the connectors extend sufficiently beyond the back side 104 of the third-level semiconductor device 100, whereby a well-bonded connection to a carrier substrate 8 is achieved.

Turning now to FIGS. 11 and 12, exemplary modes of using a plurality of first-level semiconductor devices 20 in a package 10 are illustrated.

In FIG. 11, an embodiment of a package 310 is depicted in which two or more first-level semiconductor devices 20' are positioned side-by-side within an interposer receptacle 65. The bond pads 30 of each semiconductor device 20' are flip-chip bonded by discrete conductive elements 36 to corresponding contact areas 59 on the active surface 42 of a second-level semiconductor device 40. Like the embodiments of FIGS. 8, 9 and 10, the second-level semiconductor device 40 is flip-chip bonded to the upper surface 66 of the interposer 61. FIG. 11 also illustrates an assembly structure 86, such as a film, which may be attached to the lower surface 68 of the interposer 61, covering the receptacle 65 before positioning and attaching the first-level semiconductor devices 20' in the receptacle 65. This feature is useful in assembling

packages where the first-level semiconductor devices 20′ are first mounted in the receptacle 65 of the interposer 61, followed by attachment of the second-level semiconductor device 40 to the interposer 61 and the first-level semiconductor devices 20′. The assembly structure 86 may be temporarily or permanently attached to hold one or more first-level semiconductor devices 20′ in place prior to and while electronically connecting the same to the interposer 61. The assembly structure 86 may subsequently be removed.

The embodiment of semiconductor device package 310′ shown in FIG. 12 includes a second-level semiconductor device 40 and a third-level semiconductor device 100 that are attached, flip-chip style, to the upper surface 66 and lower surface 68, respectively, of the interposer 61, as previously described. Within the interposer receptacle 65 are two first-level semiconductor devices 20A and 20B, one above the other. The upper first-level semiconductor device 20A′ is attached flip-chip style to the active surface 42 of the second-level semiconductor device 40. The lower first-level semiconductor device 20B is attached, flip-chip style, to the active surface 102 of the third-level semiconductor device 100.

In each of the figures, it is understood that the semiconductor devices (e.g., semiconductor devices 20, 40, 100, etc.) may include insulative layers (not shown) which separate electrical conductors, such as the conductive traces of redistribution layers, from each other and from other adjacent components of a package. These layers may be in the form of deposited films or preformed adhesive films that have been adhesively or otherwise secured to the semiconductor devices.

A package of the present invention which comprises two stacked semiconductor devices may have a total thickness of less than about 1 mm, making the package suitable for use in compact electronic devices, such as cellular telephones, handheld computers, and portable computers, where such low-profile packages are required or desired. In addition, the package may be formed to provide a very small footprint, e.g., about the same size as or only slightly larger than that of the second-level semiconductor device.

Several useful methods for assembling packages in accordance with teachings of the present invention are illustrated in FIGS. 13, 14 and 15.

FIGS. 13A-I depict a method for assembling a multidie semiconductor device package such as that pictured in FIGS. 2, 2A, and 2B, for example. As shown in FIG. 13A, a plurality of first-level semiconductor devices 20 is prepared on an active surface 22 of a wafer 26 or other suitable semiconductor substrate, such as a substrate formed from gallium arsenide, indium phosphide, or another semiconductive material or a so-called silicon-on-insulator (SOI) type substrate (e.g., silicon-on-glass (SOG), silicon-on-ceramic (SOC), silicon-on-sapphire (SOS), etc.). Each semiconductor device 20 typically comprises semiconductor material with internal electronic functions and a plurality of bond pads (not shown) on the active surface 22. The wafer 26 is cut along saw lines 28, as depicted in FIG. 13B, to produce individual singulated first-level semiconductor devices 20.

Likewise, as illustrated in FIG. 13C, a plurality of second-level semiconductor devices 40 is fabricated on an active surface 42 of a wafer 46 or other semiconductor substrate. These second-level semiconductor devices 40 will generally be larger in footprint than the first-level semiconductor devices 20. The wafer 46 is then cut along saw lines 48 into individual singulated second-level semiconductor devices 40, as shown in FIG. 13D.

In addition, as depicted in FIG. 13E, a plurality of interposers 61 is formed from an interposer substrate material 60. The interposer substrate 60 may be in the form of a multi-interposer sheet or strip 62, as represented in FIG. 13E, with an upper surface 66 and a lower surface 68. On one or both of the upper surface 66 and the lower surface 68 include metallization, including bond pads, contact areas, conductive traces, and/or the like, and conductive vias for vertical interconnection (not shown). Cut lines 64 are located between adjacent, individual interposers 61 of the sheet/strip 62 and form boundaries therebetween. Each interposer 61 includes a generally centrally positioned receptacle 65 formed at least partially therethrough, into which one or more first-level semiconductor devices 20 may be positioned and mounted. An assembly structure 86, such as film, may be temporarily or permanently attached to the lower surface 68 of each interposer 61 to cover the opening of the receptacle 65 thereof.

Turning now to FIG. 13F, a first-level semiconductor device 20 may be placed in each receptacle 65. The first-level semiconductor device 20 may then be electrically connected to the interposer 61 by way of intermediate conductive elements 32. This

may occur prior to separation of adjacent interposers 61 from the sheet/strip 62, as shown, or following separation of the interposers 61 from the sheet/strip 62.

Next, as shown in FIG. 13G, individual second-level semiconductor devices 40 are positioned over each receptacle 65 containing a wire-bonded first-level semiconductor device 20. Each second-level semiconductor device 40 is attached to the upper surface 66 of the interposer 61 by a dielectric adhesive material 58, such as KAPTON™ tape, for example. Intermediate conductive elements 52 may then be positioned or formed between bond pads (not shown) of the second-level semiconductor device 40 and corresponding contact areas (not shown) of the interposer 61.

As shown in FIG. 13H, encapsulation of an assembly such as that shown in FIG. 13G may be accomplished by a variety of different methods. For example, known transfer molding or pot molding processes may be used. Depending upon the particular package configuration, a preliminary step of permitting a liquid encapsulant to substantially backfill the interstitial spaces between the interposer 61 and semiconductor devices 20, 40, followed by thermal curing, will strengthen the device mounting and seal the inner spaces, enabling removal of assembly structure 86, if such is desired.

For encapsulation of packages 10 in this invention, a suitable, known type of encapsulant material 90 (e.g., a filled polymer transfer molding compound or a silicone or epoxy-type glob-top type encapsulant material) is introduced into the remaining interstitial spaces 80 within receptacle 65 of each interposer 61 of the substrate sheet/strip 62. The encapsulant material 90 extends laterally between at least portions of the outer periphery of each first-level semiconductor device 20 within the receptacle 65 and the interstitial space 80 between the second-level semiconductor device 40 and the interposer 61. The encapsulant material 90 may also substantially cover the intermediate conductive elements including all bond pads, bond wires, intermediate connectors, contact areas, and traces. Accordingly, the encapsulant material 90 may substantially fill the remaining space within receptacle 65 and at least partially cover the active surface 22, 42, 102 of each semiconductor device 20, 40, 100 as well as the regions of the upper surface 66 of the interposer 61 at which metallization areas are located.

Once the encapsulant material 90 has been introduced into the receptacle 65 and interstitial spaces 80, it is permitted or caused to harden, set, or cure. For example, if a thermoplastic resin is used as the encapsulant material 90, the encapsulant material will harden upon cooling of the same. If a transfer molding compound or other resin is used as the encapsulant material 90, the encapsulant material may be cured by the addition of a catalyst or by applying heat and/or pressure to the same. If the encapsulant material 90 is a photoimageable polymer, the encapsulant material may be set or cured by exposing the same to an appropriate wavelength of radiation.

As depicted in the figures, when encapsulant material 90 has hardened, set, or cured, the encapsulant material 90 holds the one or more first-level semiconductor devices 20 within the receptacle 65. Accordingly, an assembly structure or film 86 (FIG. 11) may be removed from the lower surface 68 of each interposer 61, with each first-level semiconductor device 20 being suspended in the receptacle 65 of that interposer 61 and the back side 24 of each first-level semiconductor device 20 within the receptacle 65 being exposed. An exemplary encapsulation of the assembly with an encapsulant material 90 in a transfer or pot mold may be used to form interconnected packages 10 of uniform size, as illustrated, or separate packages 10 that include previously separated interposers 61.

Outer connectors 18 such as balls, bumps, columns, pillars, or pins of metal or another conductive material (e.g., a conductive or conductor-filled elastomer) may be attached to contact areas of the lower surface 14 of the package 10, i.e., lower surface 68 of the interposer 61. The installation may be performed either before or after encapsulation and before or after singulation into individual packages 10, as shown in FIG. 13I. Singulation may be accomplished by use of a wafer saw or otherwise, as known in the art.

Another example of a method of the present invention, depicted in FIGS. 14A-I, is applicable to the packages shown in FIGS. 7, 8, 9, 10, 11, and 12, for example. A package formed by this method has the first-level semiconductor device 20 connected in a flip-chip manner to a second-level semiconductor device 40.

As shown in FIG. 14A, a plurality of first-level semiconductor devices 20 is prepared on an active surface 22 of a wafer 26 or other semiconductor substrate. The wafer 26 is then cut along saw lines 28, as depicted in FIG. 14B, to produce singulated

first-level semiconductor devices 20. Discrete conductive elements 36, such as balls, bumps, columns, pillars, pins, or the like, are formed secured to bond pads (not shown) of each first-level semiconductor device 20 for connection thereof to second-level semiconductor devices 40. The discrete conductive elements 36 may be attached to the bond pads of first-level semiconductor devices 20 either before or after singulation.

FIG. 14C depicts preparation of a plurality of second-level semiconductor devices 40 on a wafer 46 or other semiconductor substrate as described in reference to FIG. 13C.

As shown in FIG. 14D, a first-level semiconductor device 20 is flip-chip bonded, by discrete conductive elements 36, to the active surface 42 of each second-level semiconductor device 40 on wafer 46. Metallization (not visible) on the active surface 42 of wafer 46 connects the circuits (not visible) of both semiconductor devices 20, 40 of each two-die unit 94 (FIG. 14E) to peripheral discrete conductive elements 56, e.g., solder balls on each second-level semiconductor device 40. Wafer 46 may be cut along saw lines 48 to singulate the two-die units 94, each of which comprises a first-level semiconductor device 20 flip-chip bonded to a second-level semiconductor device 40, as shown in FIG. 14E. Alternatively, wafer 46 may be severed prior to securing or electrically connecting first-level semiconductor devices 20 to second-level semiconductor devices 40.

In FIG. 14F, a plurality of interposers 61 is shown, formed with a substrate material 60, which may comprise a sheet or strip 62 of rigid or flexible substrate material. Receptacles 65 are formed in each interposer 61 and may be located generally centrally thereon. The multi-interposer substrate sheet or strip 62 is shown in an inverted orientation, wherein outer connectors 18 are visible on the lower surface 68 of the interposer 61. Metallization (not visible), including traces 72 and contact areas 71 on the upper surface 66 of the substrate sheet or strip 62, is electrically connected to outer connectors 18 on the lower surface 68 of the interposer 61.

As shown in FIG.14G, the two-die units 94 are attached to interposers 61 of the multi-interposer substrate sheet or strip 62 by flip-chip connection of the second-level semiconductor devices 40 to the interposers 61, with the first-level semiconductor devices 20 being received by receptacles 65 of the interposers 61. As shown, first-level semiconductor devices 20 project upwardly through the receptacles 65 of the inverted

interposers 61. Each first-level semiconductor device 20 and second-level semiconductor device 40 communicates with outer connectors 18 through the intermediate conductors (bond pads, contact areas, solder balls and vias, etc.).

The assemblies shown in FIG. 14G may be collectively or individually encapsulated as shown in FIG. 14H by introducing encapsulant material 90 into the interstitial spaces 80 within receptacles 65 and underlying the second-level semiconductor device 40, which is not visible in FIG. 14H. In addition, encapsulant material 90 may cover the upper surface 66 of the interposer 61, surrounding exposed portions of the second-level semiconductor device 40. The package 10 which is illustrated in FIG. 14I is typical of packages formed by transfer molding and may include encapsulation of the interposer edges 69 (FIG. 14G) as well. Each package 10 may be singulated from the multi-interposer substrate sheet or strip 62 by cutting along lines 64 either following encapsulation, as shown in FIGS. 14H and 14I, or prior to encapsulation. The packages 10 are ready for testing and attachment to a carrier substrate 8, another package, or other apparatus.

It may be noted that the outer connectors 18 may be attached to the interposer's lower surface 68 either prior to or following attachment and electrical connection of the semiconductor devices 20 and 40 to the interposer 61.

Another exemplary method for assembly of a package 10 in accordance with the teachings of the present invention is illustrated in FIGS. 15A-15K. As shown in FIG. 15A, a plurality of second-level semiconductor devices 40 is fabricated on an active surface 42 of a wafer 46 or other semiconductor substrate. Individual second-level semiconductor devices 40 are delineated by saw lines 48 on the wafer 46. In FIG. 15B, wafer 46 is cut along saw lines 48 into individual second-level semiconductor devices 40. Discrete conductive elements 56 are placed on bond pads (not shown) on the active surface 42 while the second-level semiconductor devices 40 remain part of wafer 46 or following singulation of second-level semiconductor devices 40 from the wafer 46.

As depicted in FIG. 15C, a plurality of interposers 61 is formed with substrate material 60 in the form of a multi-interposer sheet or strip 62. The sheet/strip 62 is formed of suitable material 60 of any desired rigidity or flexibility. The sheet/strip 62

has an upper surface 66 and a lower surface 68. A receptacle 65 is formed in each interposer 61, extending between the upper and lower surfaces 66 and 68.

Once interposers 61 and second-level semiconductor devices 40 have been fabricated, second-level semiconductor devices 40 are mounted, flip-chip style, to the upper surface 66 of each interposer 61 of the sheet/strip 62, with each second-level semiconductor device 40 at least partially covering a receptacle 65, as depicted in FIG. 15D. The sheet/strip 62 is shown in FIG. 15E in an inverted orientation. Outer connectors 18 protrude visibly from the lower surface 68 of each interposer 61. These outer connectors 18 may be applied to the sheet/strip 62 either before or after attachment and/or electrical connection of the second-level semiconductor devices 40 thereto.

Continuing the assembly process, as shown in FIG. 15F, a plurality of first-level semiconductor devices 20 is formed on an active surface 22 of wafer 26 or other semiconductor substrate, as previously described with reference to FIG. 13A. Discrete conductive elements 36 are attached to bond pads (not shown) on the active surfaces 22 of the first-level semiconductor devices 20. Next, as illustrated in FIG. 15G, the wafer 26 is cut along saw lines 28 to singulate first-level semiconductor devices 20 from one another.

Turning now to FIG. 15H, first-level semiconductor devices 20 are inverted, positioned at least partially within receptacles 65 of interposers 61, and bonded, flip-chip style, to the active surfaces 42 (not shown) of the second-level semiconductor devices 40. Interstitial spaces 80 are located around each first-level semiconductor device 20, between semiconductor devices 20 and 40, and between semiconductor devices 20, 40 and the interposers 61.

As shown in FIG. 15I, encapsulant material 90 may be introduced into interstitial spaces 80, as well as around second-level semiconductor devices 40.

The encapsulated structure of FIG. 15I may be cut along cut lines 64 to form singulated packages 10. Alternatively, singulation may be effected prior to encapsulation. Each package 10 includes an upper surface 12 and a lower surface 14, which are identified in the respective upper and lower views of package 10 of FIGS. 15J and 15K. The packaging configuration is typical of that produced by known transfer molding or pot molding processes. Optionally, the encapsulation step may be

configured to cover the exposed back sides of second-level semiconductor device 40 and/or first-level semiconductor device 20. Optionally, any bare edges of the interposer, i.e., those exposed at cut lines 64, may be covered by an encapsulant in a subsequent step. The edges may be covered by an encapsulant, e.g., glob top, at the time that the package 10 is mounted on a carrier substrate.

Where additional semiconductor devices, e.g., semiconductor device 100, are to be mounted on an interposer 61, relevant portions of the described methods may be repeated for each semiconductor device or device combination to achieve the desired package configuration.

With returned reference to FIG. 5, formation of package stacks 88 requires a further step of bonding or otherwise securing packages 10 to each other. Further encapsulation may be performed to enclose outer connectors 18A of the upper package(s) 110'.

While the above methods are illustrated with the outer connectors 18 arranged in BGA connection patterns, other arrangements and types of conductive elements may also be used to connect a package 10 to a carrier substrate 8, another package or other apparatus. For example, bumps, columns, bonded leads or tape-automated bond (TAB) elements may be used, as may plug-in type connectors and others known in the art. Likewise, other types of discrete conductive elements 36, 56, 116 may be used to connect semiconductor devices 20, 40, 100 to each other or to the interposer 61.

The overall thickness of the resulting semiconductor device package 10 is substantially equal to the combined thicknesses of the interposer 61 and the second-level semiconductor device 40, and the distance of outer connectors 18 from the lower surface 68 of interposer 61. The thickness of a third-level semiconductor device 100 does not contribute to the overall package thickness, being positioned between the outer connectors 18.

While the figures depict the inventive process using a substrate sheet/strip 62 having a plurality of physically connected interposers 61, each interposer 61 having a single receptacle 65 with one or more first-level semiconductor devices 20 mounted therein, it will be understood that the process is applicable to any interposer 61 with a receptacle 65 extending substantially therethrough, including an interposer 61 having more than one receptacle 65.

Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of some exemplary embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. Features from different embodiments may be employed in combination. The scope of the invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions, and modifications to the invention, as disclosed herein, which fall within the meaning and scope of the claims are to be embraced thereby.

CLAIMS

What is claimed is:

1. A semiconductor device assembly, comprising:

an interposer including at least one receptacle configured to at least partially receive a semiconductor device formed therein;

at least one semiconductor device positioned at least partially within and at least partially laterally confined within said at least one receptacle; and

at least another semiconductor device at least partially superimposed over said at least one semiconductor device and at least partially supported by said interposer.

2. The semiconductor device assembly of claim 1, wherein said at least one receptacle extends substantially through said interposer.

3. The semiconductor device assembly of claim 1, wherein said at least one semiconductor device is completely laterally surrounded by said interposer.

4. The semiconductor device assembly of claim 1, wherein active surfaces of said at least one semiconductor device and said at least another semiconductor device face in substantially the same direction.

5. The semiconductor device assembly of claim 4, further comprising:

at least one intermediate conductive element extending laterally between and electrically connecting a bond pad of said at least one semiconductor device to a corresponding contact area of said interposer; and

at least another intermediate conductive element extending laterally between and electrically connecting a bond pad of said at least another semiconductor device and another corresponding contact area of said interposer.

6. The semiconductor device assembly of claim 5, wherein said corresponding contact area and said another corresponding contact area are located on the same surface of said interposer.

7. The semiconductor device assembly of claim 4, wherein said at least another semiconductor device includes at least one redistribution circuit on a surface thereof.

8. The semiconductor device assembly of claim 7, further comprising:

at least one discrete conductive element electrically connecting a bond pad of said at least one semiconductor device and a portion of said at least one redistribution circuit in alignment with said bond pad; and

at least another discrete conductive element electrically connecting another portion of said at least one redistribution circuit and a corresponding contact area of said interposer in alignment with said another portion.

9. The semiconductor device assembly of claim 8, wherein said at least one redistribution circuit is carried upon a back side of said at least another semiconductor device.

10. The semiconductor device assembly of claim 9, further comprising:

at least one intermediate conductive element extending laterally between and electrically connecting a bond pad on said active surface of said at least another semiconductor device and another corresponding contact area of said interposer.

11. The semiconductor device assembly of claim 8, wherein said at least one redistribution circuit is carried upon said active surface of said at least another semiconductor device.

12. The semiconductor device assembly of claim 11, further comprising:

at least another discrete conductive element electrically connecting a bond pad on said active surface of said at least another semiconductor device and another corresponding contact area of said interposer in substantial alignment with said bond pad.

13. The semiconductor device assembly of claim 1, wherein active surfaces of said at least one semiconductor device and said at least another semiconductor device face one another.

14. The semiconductor device assembly of claim 13, further comprising:

at least one discrete conductive element extending between and electrically connecting a bond pad of said at least one semiconductor device and a corresponding bond pad of said at least another semiconductor device in substantially alignment with said bond pad; and

at least another discrete conductive element extending between and electrically connecting another bond pad of said at least another semiconductor device and a corresponding contact area of said interposer in substantial alignment with said another bond pad.

15. The semiconductor device assembly of claim 14, wherein said corresponding bond pad of said at least another semiconductor device comprises a portion of a redistribution circuit on said active surface of said at least another semiconductor device.

16. The semiconductor device assembly of claim 15, wherein said redistribution circuit further comprises a circuit trace in communication with said corresponding bond pad and a redistribution bond pad at an opposite end of said circuit trace.

17. The semiconductor device assembly of claim 16, wherein said another bond pad of said at least another semiconductor device comprises said redistribution bond pad.

18. The semiconductor device assembly of claim 13, comprising at least two semiconductor devices positioned at least partially within said at least one receptacle.

19. The semiconductor device assembly of claim 18, wherein back sides of said at least two semiconductor devices face one another.

20. The semiconductor device assembly of claim 19, wherein another semiconductor device is positioned adjacent to an active surface of each of said at least two semiconductor devices.

21. The semiconductor device assembly of claim 1, wherein:

circuitry of said at least another semiconductor device is in electrical communication with corresponding circuitry of said interposer; and

circuitry of said at least one semiconductor device is in electrical communication with corresponding circuitry of at least one of said at least another semiconductor device and said interposer.

22. The semiconductor device assembly of claim 21, further comprising:

a quantity of underfill material between at least peripheral edges of said at least one semiconductor device and surfaces of said at least one receptacle.

23. The semiconductor device assembly of claim 22, wherein said underfill material is located between adjacent surfaces of said at least one semiconductor device and said at least another semiconductor device.

24. The semiconductor device assembly of claim 21, further comprising:

encapsulant material covering at least a peripheral edge of said at least another semiconductor device and adjacent regions of said interposer.

25. The semiconductor device assembly of claim 21, further comprising:
conductive structures on said interposer for electrical connection of said interposer to a higher-level substrate.

26. The semiconductor device assembly of claim 25, wherein said conductive structures comprise contact pads on a surface of said interposer and discrete conductive elements that protrude from said surface of said interposer.

27. The semiconductor device assembly of claim 26, wherein said discrete conductive elements protrude from an opposite surface from that by which said at least another semiconductor device is at least partially supported.

28. The semiconductor device assembly of claim 26, wherein said discrete conductive elements protrude from the same surface as that by which said at least another semiconductor device is at least partially supported.

29. The semiconductor device assembly of claim 26, wherein said discrete conductive elements comprise at least one of balls, bumps, columns, pillars, and pins of conductive material.

30. The semiconductor device assembly of claim 1, wherein said interposer includes:
first contact pads on a first surface thereof for establishing electrical communication between circuitry of said interposer or a semiconductor device supported thereby and a higher-level substrate; and
second contact pads on a second surface thereof, opposite said first surface, for establishing electrical communication between said circuitry of said interposer or said semiconductor device supported thereby and another semiconductor device assembly at least partially superimposed over said interposer.

31. A semiconductor device assembly, comprising:

an interposer including a first surface, a second surface opposite said first surface, and at least one receptacle extending from said first surface to said second surface;

a first semiconductor device positioned at least partially adjacent to said first surface and including an active surface, at least a portion of which faces said at least one receptacle;

at least one first discrete conductive element electrically connecting a bond pad of said first semiconductor device and a corresponding contact pad at said first surface of said interposer that is in substantial alignment with said bond pad;

a second semiconductor device positioned at least partially adjacent to said second surface and including an active surface, at least a portion of which faces said at least one receptacle; and

at least one second discrete conductive element electrically connecting a bond pad of said second semiconductor device and a corresponding bond pad of said first semiconductor device through said at least one receptacle.

32. The semiconductor device assembly of claim 31, wherein said at least one second discrete conductive element comprises at least one of a ball, bump, column, pillar, and pin.

33. The semiconductor device assembly of claim 31, wherein said corresponding bond pad comprises a portion of a redistribution circuit on said active surface of said first semiconductor device.

34. The semiconductor device assembly of claim 33, wherein said redistribution circuit further comprises a conductive trace in electrical communication with said corresponding bond pad and a redistribution bond pad at an end of said conductive trace opposite from said corresponding bond pad.

35. The semiconductor device assembly of claim 34, wherein said redistribution bond pad is positioned adjacent to an outer periphery of said second semiconductor device.

36. A multidie semiconductor device package, comprising:

an interposer, comprising:

a substrate with upper and lower surfaces;

a receptacle extending between said upper and lower surfaces; and

electrical conductors on at least said upper surface;

at least one first-level semiconductor device positioned within said receptacle, each said at least one first-level semiconductor device having an active surface;

a second-level semiconductor device positioned above said upper surface of said substrate and attached thereto, said second-level semiconductor device having an active surface; and

electrical connections connecting said at least one first-level semiconductor device and said second-level semiconductor device to said electrical conductors.

37. The multidie semiconductor device package of claim 36, further comprising outer connectors for attaching said multidie semiconductor device package to conductors on an object.

38. The multidie semiconductor device package of claim 37, wherein said outer connectors are mounted on said lower surface of said substrate and conductively connected to said electrical conductors.

39. The multidie semiconductor device package of claim 38, wherein said outer connectors are conductively connected to said electrical conductors by conductive vias extending between said upper surface and said lower surface of said substrate.

40. The multidie semiconductor device package of claim 37, wherein said object comprises one of a circuit board and another semiconductor device package.

41. The multidie semiconductor device package of claim 37, wherein said outer connectors comprise one of conductive balls, conductive bumps, conductive columns, conductive pins and plug-in type electrical connectors.

42. The multidie semiconductor device package of claim 36, wherein said second-level semiconductor device has a larger footprint than that of said at least one first-level semiconductor device.

43. The multidie semiconductor device package of claim 36, wherein said second-level semiconductor device is larger than said receptacle in at least one of an X and Y dimension.

44. The multidie semiconductor device package of claim 36, wherein said electrical connections connecting said at least one first-level semiconductor device to said electrical conductors comprise elongate, intermediate conductive elements.

45. The multidie semiconductor device package of claim 36, wherein said electrical connections connecting said second-level semiconductor device to said electrical conductors comprise elongate, intermediate conductive elements.

46. The multidie semiconductor device package of claim 36, wherein said electrical connections connecting said second-level semiconductor device to said electrical conductors comprise discrete conductive elements interposed between said active surface of said second-level semiconductor device and said electrical conductors.

47. The multidie semiconductor device package of claim 46, wherein said electrical connections connecting said second-level semiconductor device to said electrical conductors comprise one of conductive balls, conductive bumps, conductive pins, conductive columns, conductive pillars, and conductive regions of z-axis conductive or conductor-filled elastomer.

48. The multidie semiconductor device package of claim 46, wherein bond pads of said at least one first-level semiconductor device are connected to corresponding bond pads on said active surface of said second-level semiconductor device by first-level electrical connections.

49. The multidie semiconductor device package of claim 48, wherein said first-level electrical connections between said bond pads of said at least one first-level semiconductor device and said corresponding bond pads of said second-level semiconductor device comprise one of conductive balls, conductive bumps, conductive pins, conductive columns, conductive pillars and conductive regions of z-axis conductive or conductor-filled elastomer.

50. The multidie semiconductor device package of claim 46, wherein said second-level semiconductor device is attached to said upper surface of said substrate of said interposer.

51. The multidie semiconductor device package of claim 36, wherein a back side of said at least one first-level semiconductor device is substantially coplanar with said lower surface of said substrate.

52. The multidie semiconductor device package of claim 36, further comprising a third-level semiconductor device with an active surface, bond pads on said active surface of said third-level semiconductor device being attached by conductive connectors to said lower surface of said substrate.

53. The multidie semiconductor device package of claim 52, wherein said conductive connectors on said third-level semiconductor device comprise one of conductive balls, conductive bumps, conductive pins, conductive columns, conductive pillars, conductive regions of z-axis conductive or conductor-filled elastomer, bond wires, conductive tape-automated bonding elements, and leads.

54. The multidie semiconductor device package of claim 52, further comprising a second first-level semiconductor device positioned below said at least one first-level semiconductor device in said receptacle, said second first-level semiconductor device electrically attached to said third-level semiconductor device in a flip-chip arrangement.

55. The multidie semiconductor device package of claim 36, wherein said at least one first-level semiconductor device comprises a plurality of first-level semiconductor devices mounted side-by-side in said receptacle.

56. A method for assembling a multidie semiconductor device package, comprising:

providing an interposer with a substantially planar substrate and a receptacle formed substantially through said substrate, said substrate having an upper surface and a lower surface, at least said upper surface having conductors thereon;

positioning at least one first-level semiconductor device within said receptacle, an interstitial space remaining at least between peripheral edges of said at least one first-level semiconductor device and said substrate;

positioning a second-level semiconductor device above said upper surface of said substrate;

electrically connecting said at least one first-level semiconductor device to at least one of said conductors on said upper surface of said substrate and said second-level semiconductor device by first-level conductive members; and

electrically connecting said second-level semiconductor device to said conductors on said upper surface of said substrate by second-level conductive members.

57. The method of claim 56, further comprising introducing a quantity of encapsulant material into said receptacle so as to fill at least a portion of said interstitial space.

58. The method of claim 56, wherein said introducing encapsulant material is effected after said electrically connecting said at least one first-level semiconductor device.

59. The method of claim 57, further comprising introducing a quantity of encapsulant material between said second-level semiconductor device and said at least one first-level semiconductor device.

60. The method of claim 56, wherein said electrically connecting said at least one first-level semiconductor device comprises forming or positioning intermediate conductive elements between bond pads of said at least one first-level semiconductor device and corresponding conductors of said interposer.

61. The method of claim 56, wherein said electrically connecting said second-level semiconductor device comprises forming or positioning intermediate conductive elements between bond pads of said second-level semiconductor device and corresponding conductors of said interposer.

62. The method of claim 56, wherein said positioning said second-level semiconductor device comprises at least one of positioning said second-level semiconductor device in a flip-chip arrangement over said at least one first-level semiconductor device and positioning said second-level semiconductor device over said interposer.

63. The method of claim 62, wherein said at least one first-level semiconductor device and said second-level semiconductor device are secured to one another before said positioning said second-level semiconductor device.

64. The method of claim 56, wherein said providing an interposer comprises providing a multi-interposer substrate on which said at least one first-level semiconductor device and said second-level semiconductor device are positioned and electrically connected.

65. The method of claim 64, further comprising singulating individual assemblies or packages from said multi-interposer substrate.

66. The method of claim 57, further comprising adhering a film to said lower surface of said substrate to cover at least a portion of said receptacle prior to positioning said at least one first-level semiconductor device therein.

67. The method of claim 66, further comprising removing said adhered film from said lower surface following curing of said encapsulant in said receptacle.