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DELAY CIRCUIT FOR RING OSCILLATOR

ABSTRACT

There is disclosed a delay circuit for a ring oscillator having output lines (2A, 2B) a pair of first transistors (MP1, MP2) arranged between the first potential line (VDD) and the output lines (2A, 2B) respectively. A second electric potential line (5) and a pair of second transistors (MN1, MN2) are arranged between the second electric potential line (5) and the output lines (2A, 2B), respectively. Respective gates of the first transistors (MP1, MP2) are connected to the output lines (2A, 2B), respectively. The first transistor (MP1, MP2), and the second transistor (MN1, MN2) are connected to each other center-symmetrically, and the output lines (2A, 2B) are connected to a third electric potential line. This circuit can realize a differential gain ≥ 1 and an inphase gain ≤ 1 .

FIG 1