17 MAY 2004

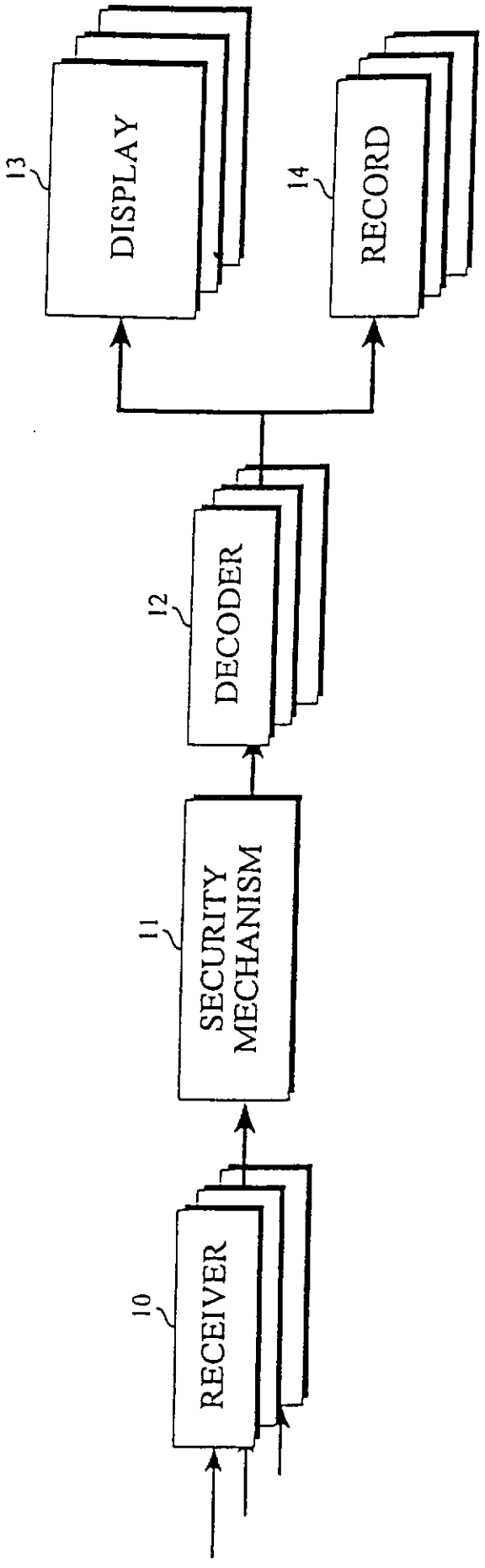


Fig. 1

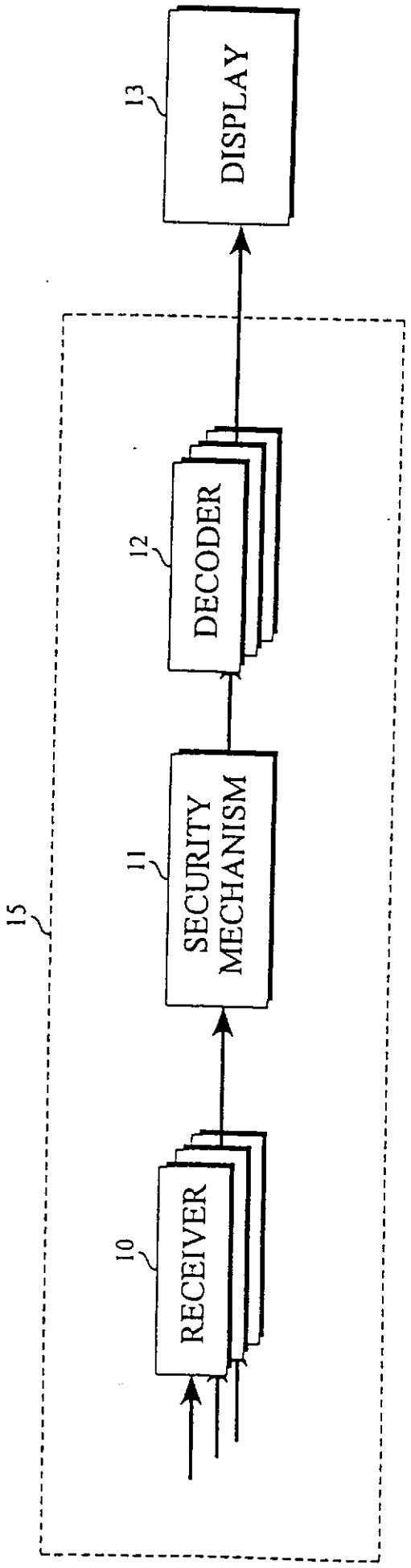

15
10
RECEIVER
11
SECURITY MECHANISM
12
DECODER
13
DISPLAY

Fig. 2A

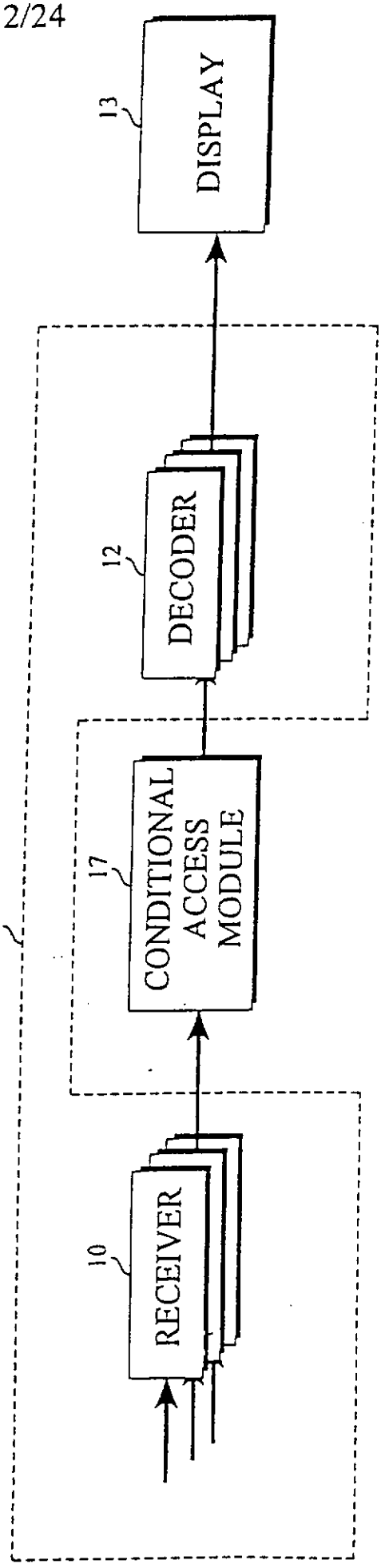

16
10
RECEIVER
17
CONDITIONAL ACCESS MODULE
12
DECODER
13
DISPLAY

Fig. 2B

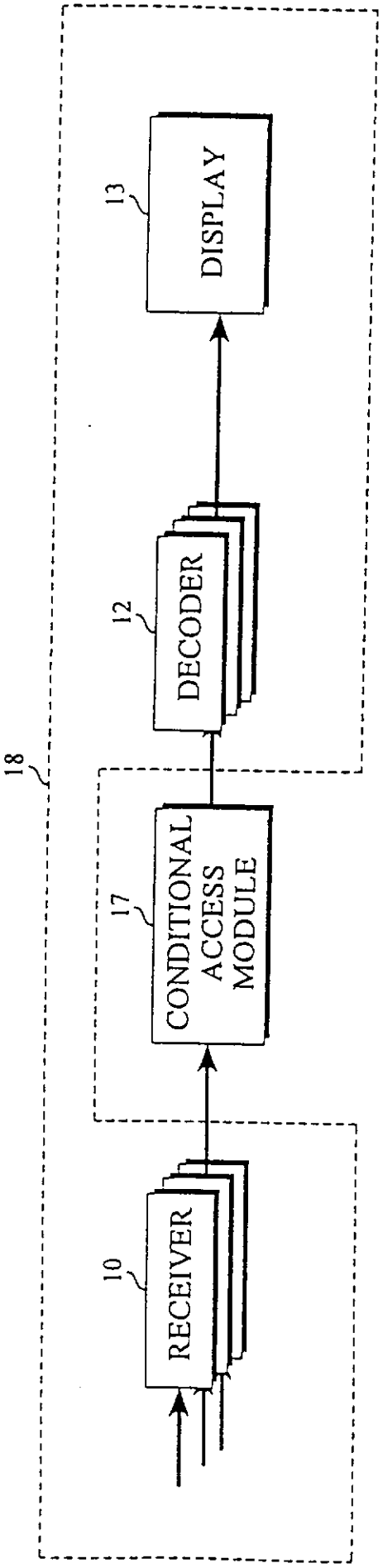

18
13
DISPLAY
12
DECODER
17
CONDITIONAL ACCESS MODULE
10
RECEIVER

Fig. 2C

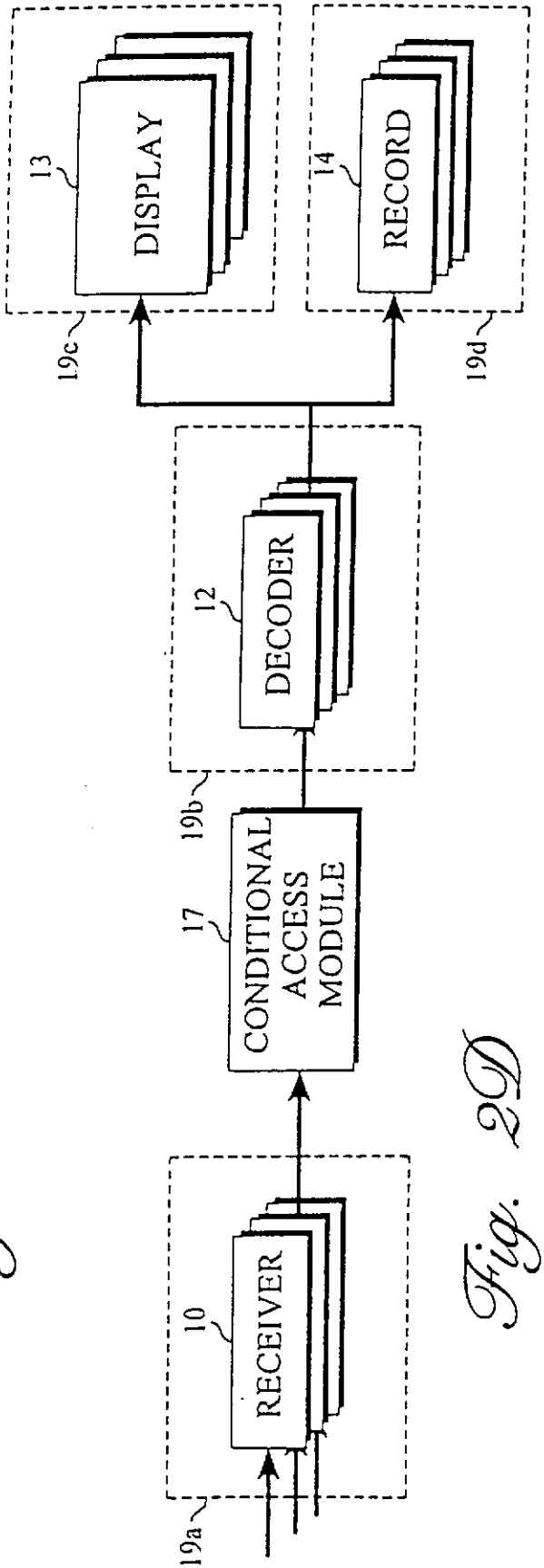

13
DISPLAY
14
RECORD
19c
19d
12
DECODER
19b
17
CONDITIONAL ACCESS MODULE
10
RECEIVER
19a

Fig. 2D

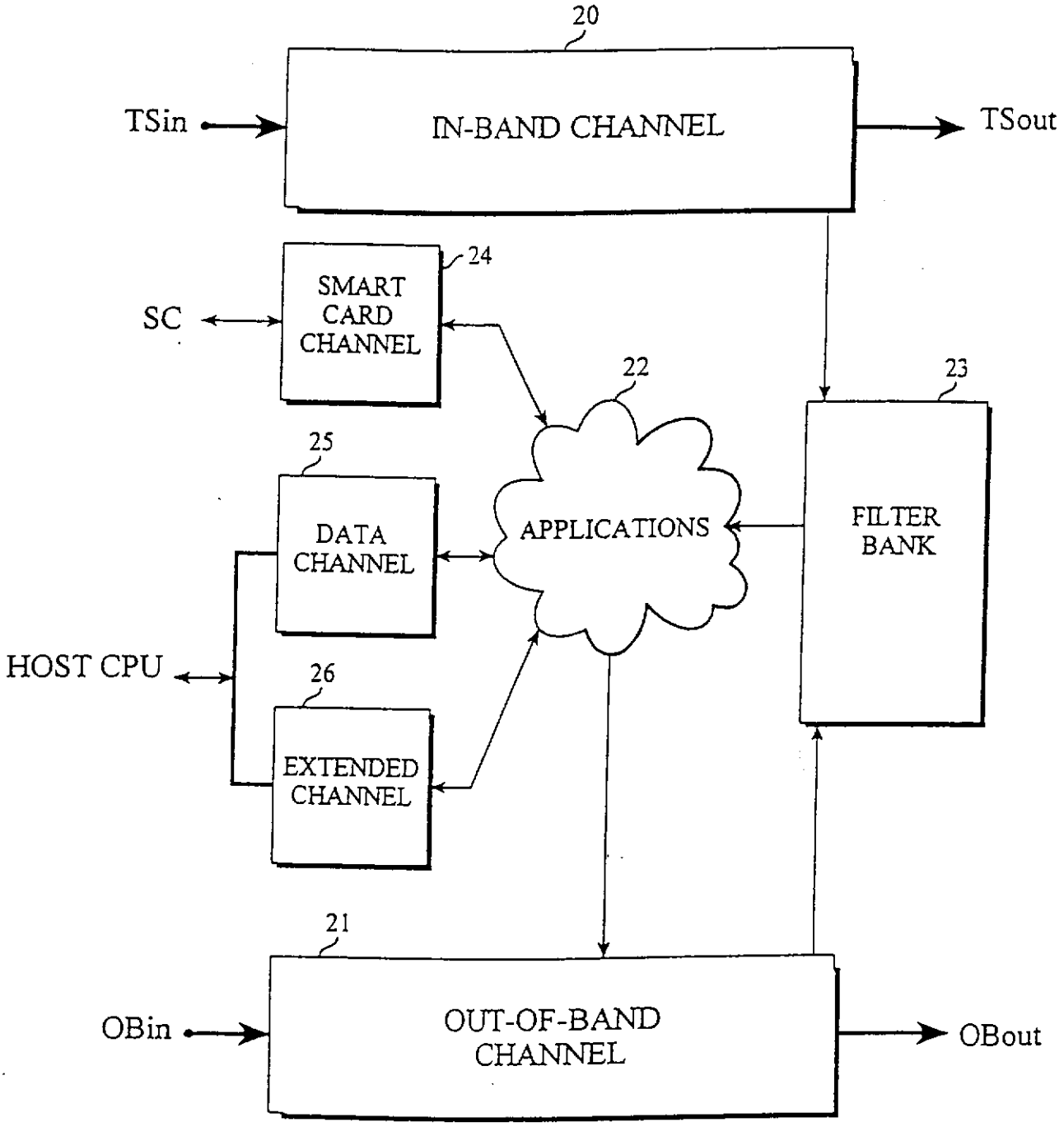

20
TSin
IN-BAND CHANNEL
TSout
24
SMART CARD CHANNEL
SC
22
23
25
DATA CHANNEL
APPLICATIONS
FILTER BANK
HOST CPU
26
EXTENDED CHANNEL
21
OBin
OUT-OF-BAND CHANNEL
OBout

Fig. 3

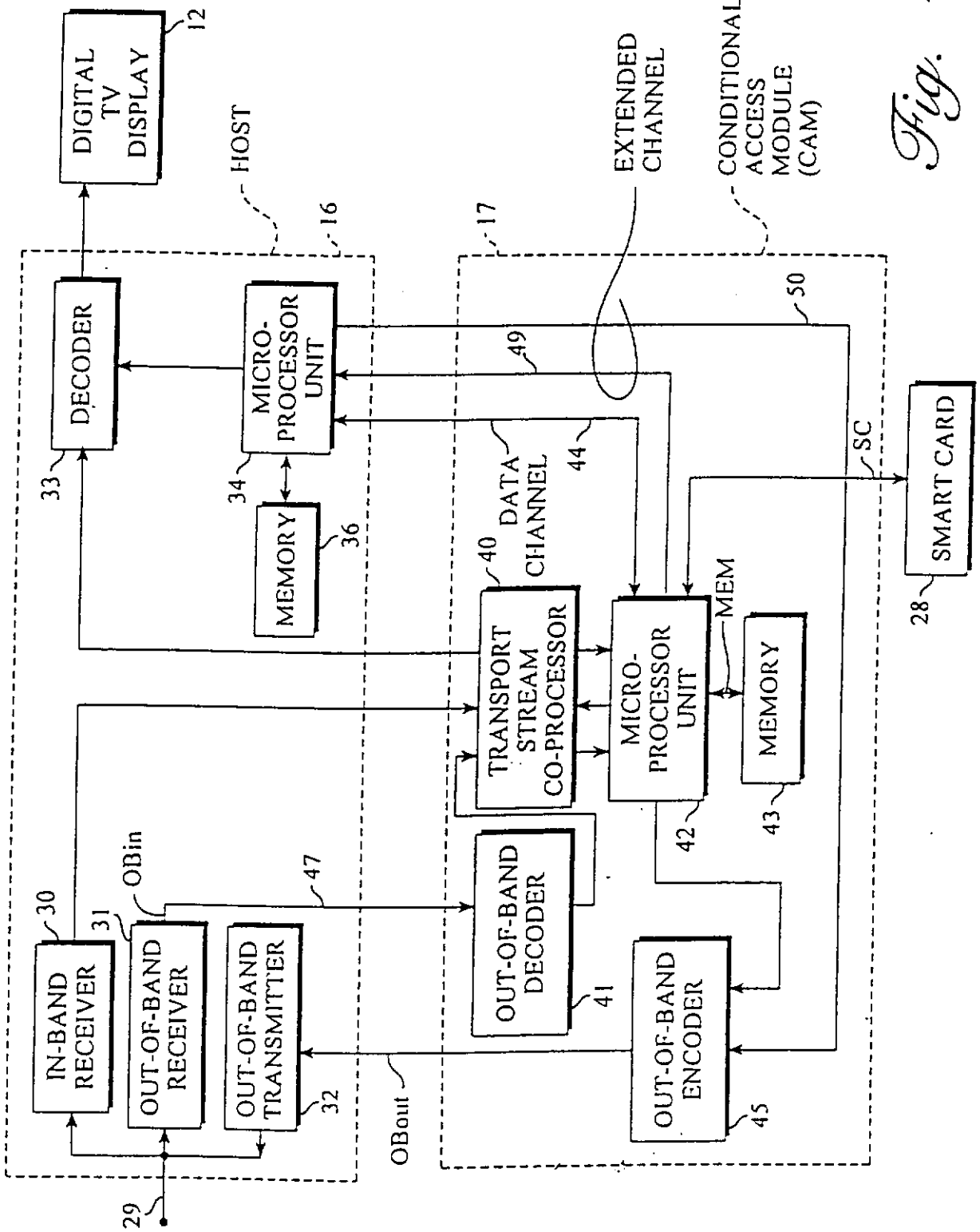

DIGITAL TV DISPLAY
12
HOST
16
17
EXTENDED CHANNEL
CONDITIONAL ACCESS MODULE (CAM)
DECODER
MICRO-PROCESSOR UNIT
50
49
33
34
44
DATA CHANNEL
SC
SMART CARD
28
MEMORY
36
40
TRANSPORT STREAM CO-PROCESSOR
MICRO-PROCESSOR UNIT
MEM
MEMORY
43
42
OBin
30
31
47
IN-BAND RECEIVER
OUT-OF-BAND RECEIVER
OUT-OF-BAND TRANSMITTER
OUT-OF-BAND DECODER
41
OUT-OF-BAND ENCODER
45
32
OBout
29

Fig. 4

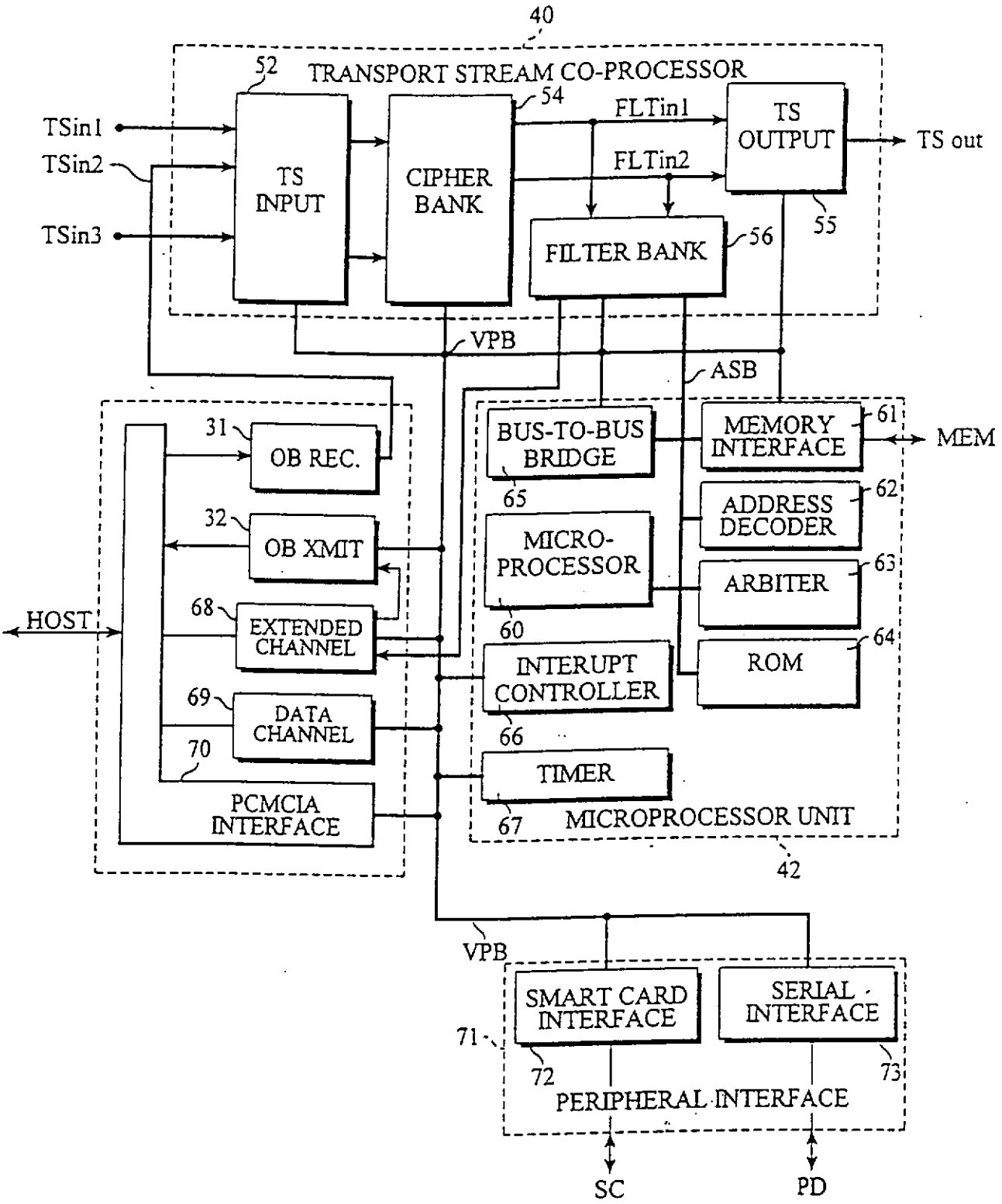

40
TRANSPORT STREAM CO-PROCESSOR
52
TSin1
TSin2
TSin3
TS INPUT
CIPHER BANK
54
FLTin1
FLTin2
TS OUTPUT
TS out
55
FILTER BANK
56
VPB
ASB
31
OB REC.
32
OB XMIT
68
EXTENDED CHANNEL
69
DATA CHANNEL
70
PCMCIA INTERFACE
HOST
BUS-TO-BUS BRIDGE
65
MICRO-PROCESSOR
60
INTERUPT CONTROLLER
66
TIMER
67
MEMORY INTERFACE
61
MEM
ADDRESS DECODER
62
ARBITER
63
ROM
64
MICROPROCESSOR UNIT
42
VPB
SMART CARD INTERFACE
71
72
SERIAL INTERFACE
73
PERIPHERAL INTERFACE
SC
PD

Fig. 5

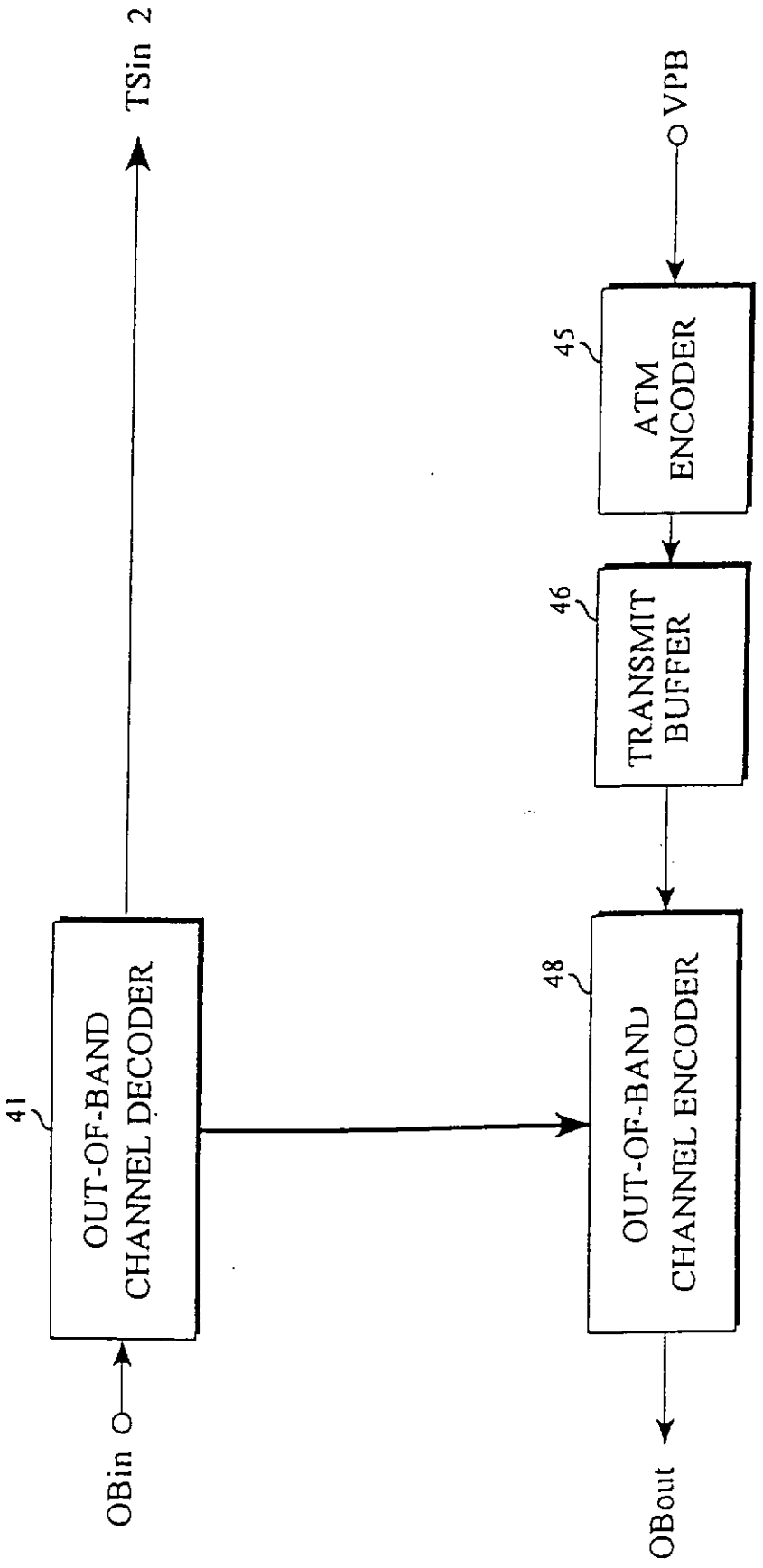

TSin 2
VPB
45
ATM ENCODER
46
TRANSMIT BUFFER
41
OUT-OF-BAND CHANNEL DECODER
48
OUT-OF-BAND CHANNEL ENCODER
OBin
OBout

Fig. 6

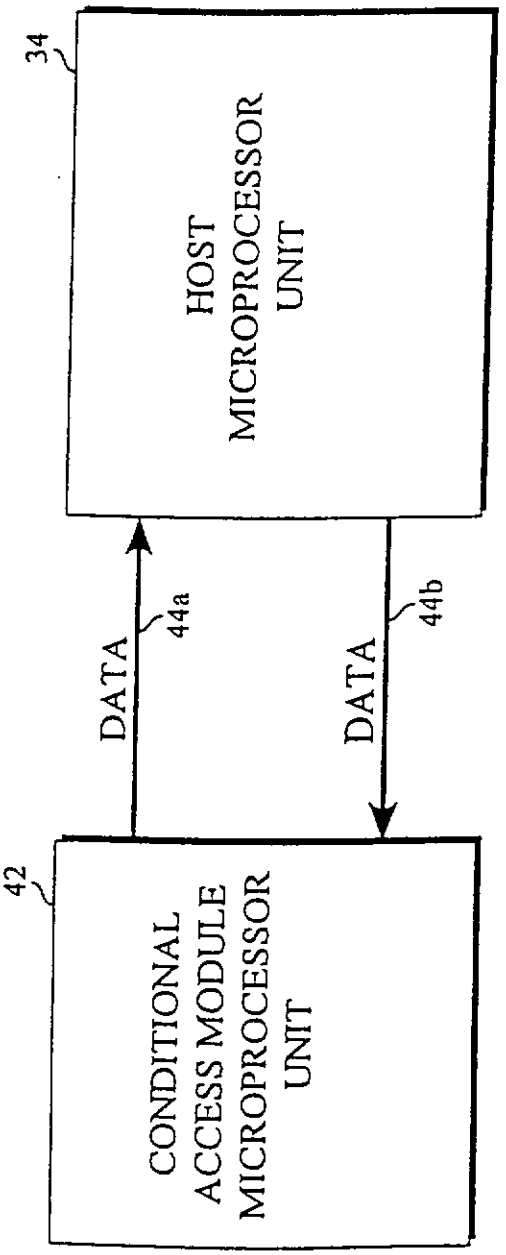

34
HOST
MICROPROCESSOR
UNIT
DATA
44a
DATA
44b
42
CONDITIONAL
ACCESS MODULE
MICROPROCESSOR
UNIT

Fig. 7

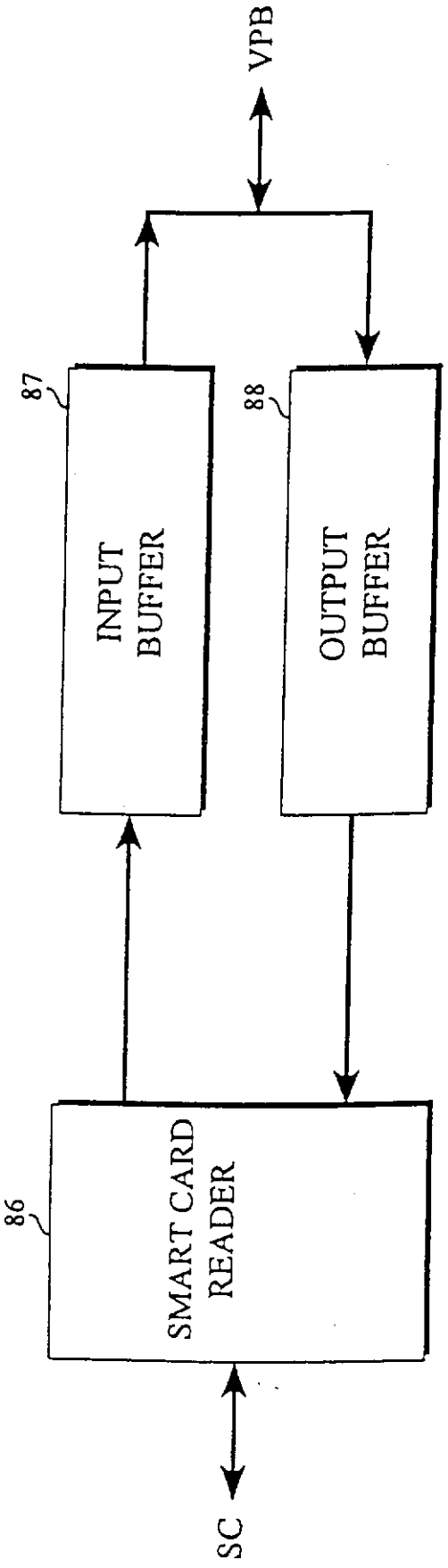


Fig. 8

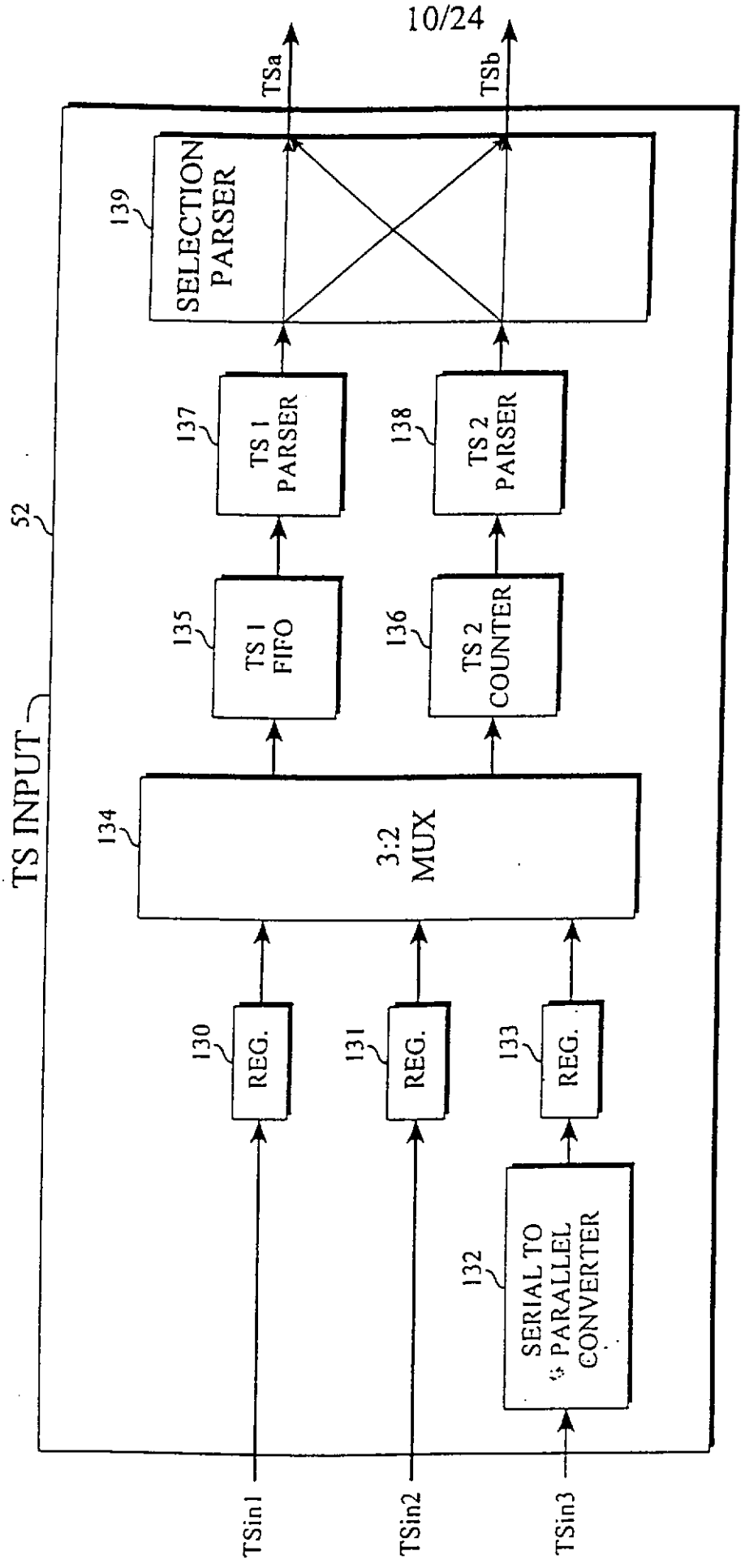

TSa
TSb
139
SELECTION PARSER
137
TS 1 PARSER
138
TS 2 PARSER
52
135
TS 1 FIFO
136
TS 2 COUNTER
TS INPUT
134
3:2 MUX
130
REG.
131
REG.
133
REG.
132
SERIAL TO PARALLEL CONVERTER
TSin1
TSin2
TSin3

Fig. 9

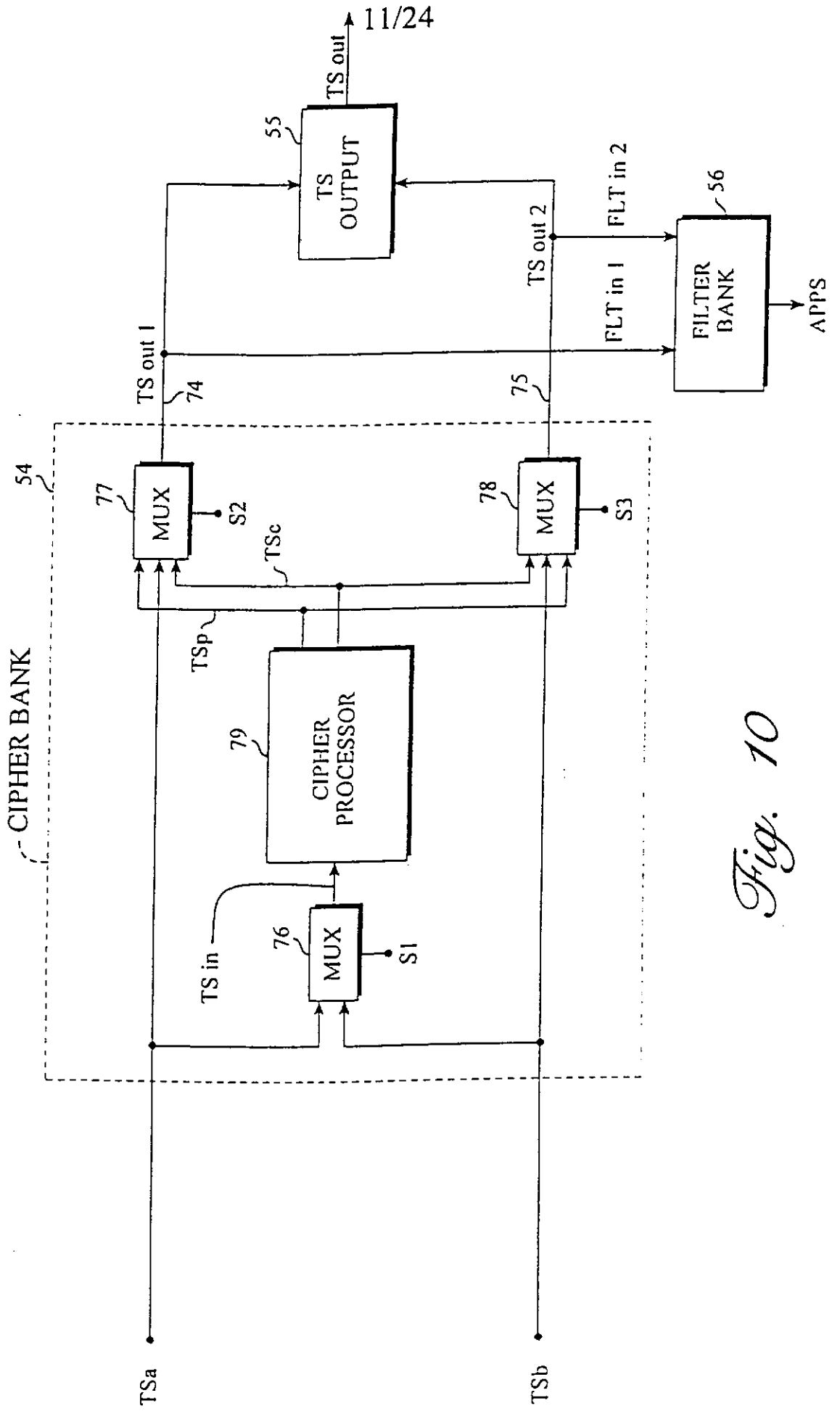

TS out
55
TS OUTPUT
TS out 2
FLT in 2
56
FLT in 1
FILTER BANK
APPS
TS out 1
74
75
54
77
MUX
S2
TSc
78
MUX
S3
TSp
CIPHER BANK
79
CIPHER PROCESSOR
TS in
76
MUX
S1
TSa
TSb

Fig. 10

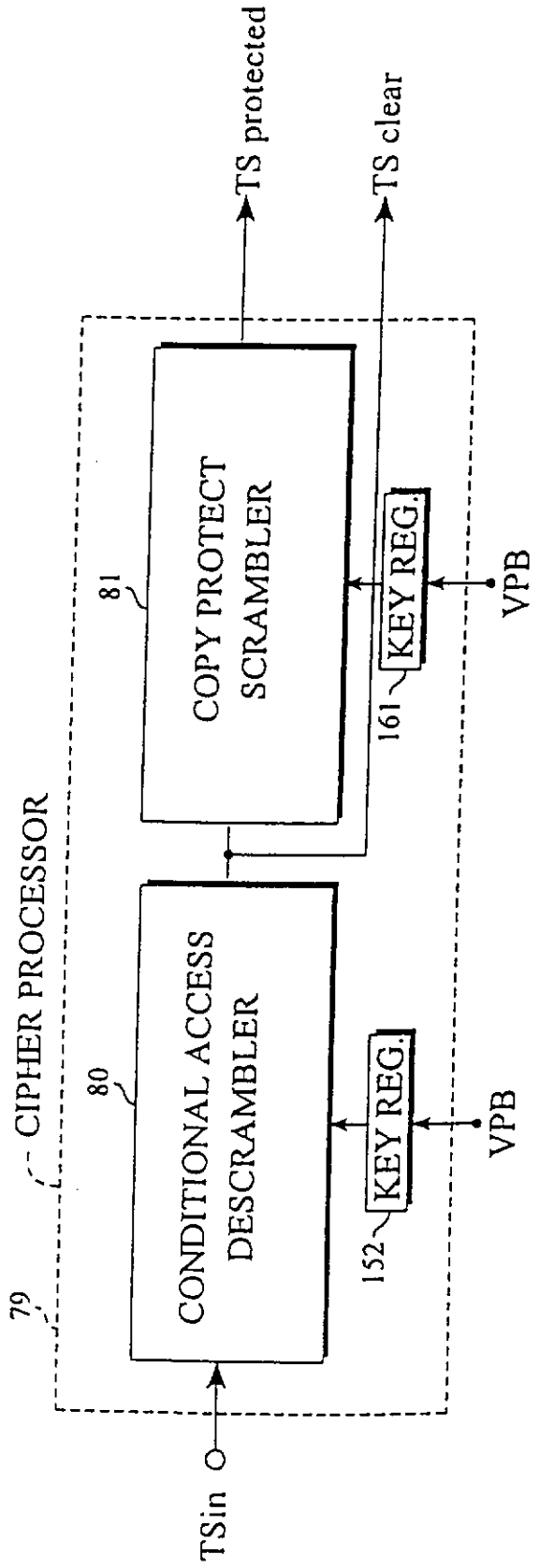

TS protected
TS clear
CIPHER PROCESSOR
81
COPY PROTECT SCRAMBLER
161
KEY REG.
VPB
80
CONDITIONAL ACCESS DESCRAMBLER
152
KEY REG.
VPB
79
TSin

Fig. 11

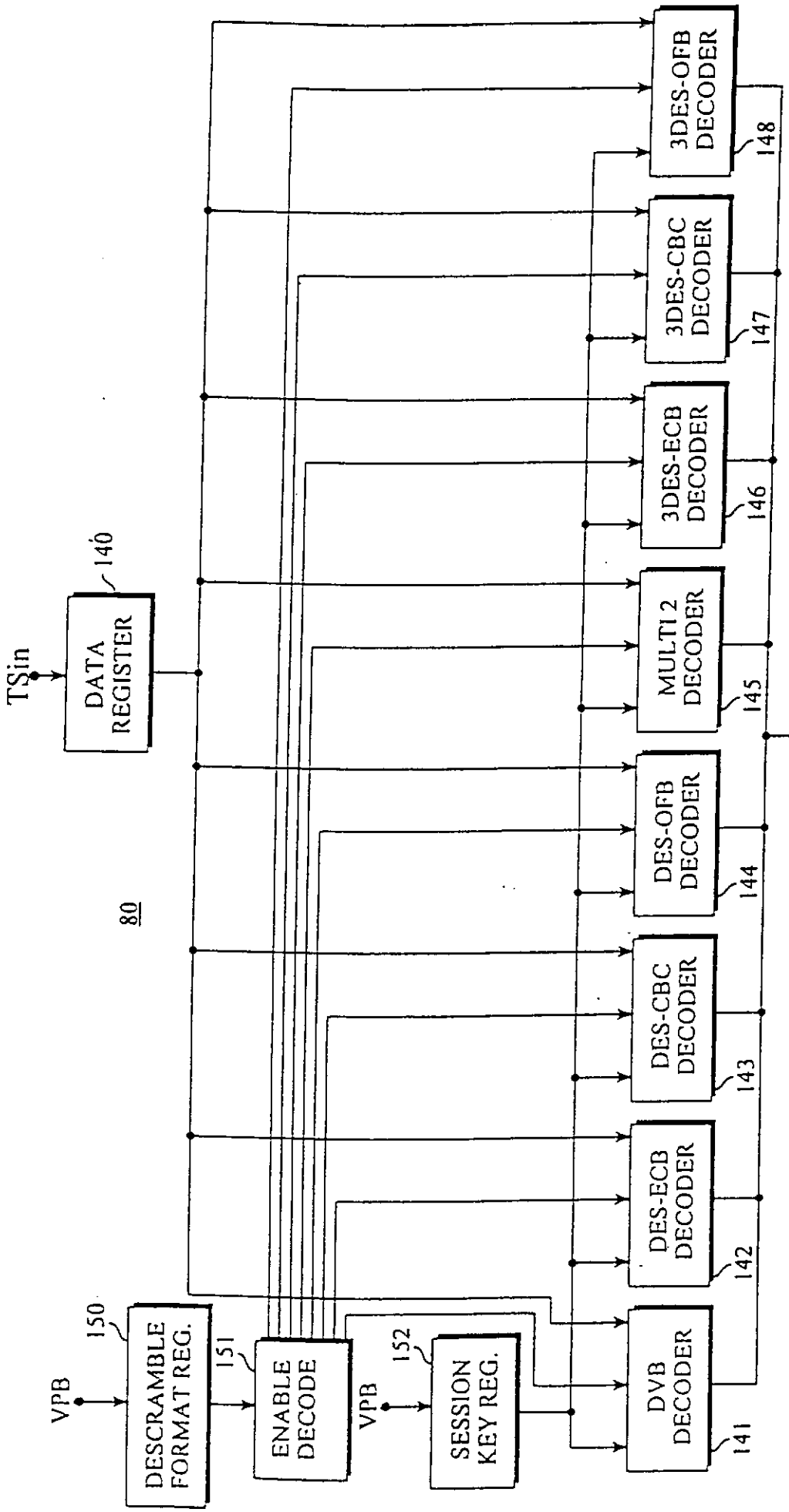

80
TSin
140
DATA REGISTER
VPB
150
DESCRAMBLE FORMAT REG.
151
ENABLE DECODE
VPB
152
SESSION KEY REG.
DVB DECODER
141
DES-ECB DECODER
142
DES-CBC DECODER
143
DES-OFB DECODER
144
MULTI 2 DECODER
145
3DES-ECB DECODER
146
3DES-CBC DECODER
147
3DES-OFB DECODER
148
153
DATA REGISTER
TSclear

Fig. 12

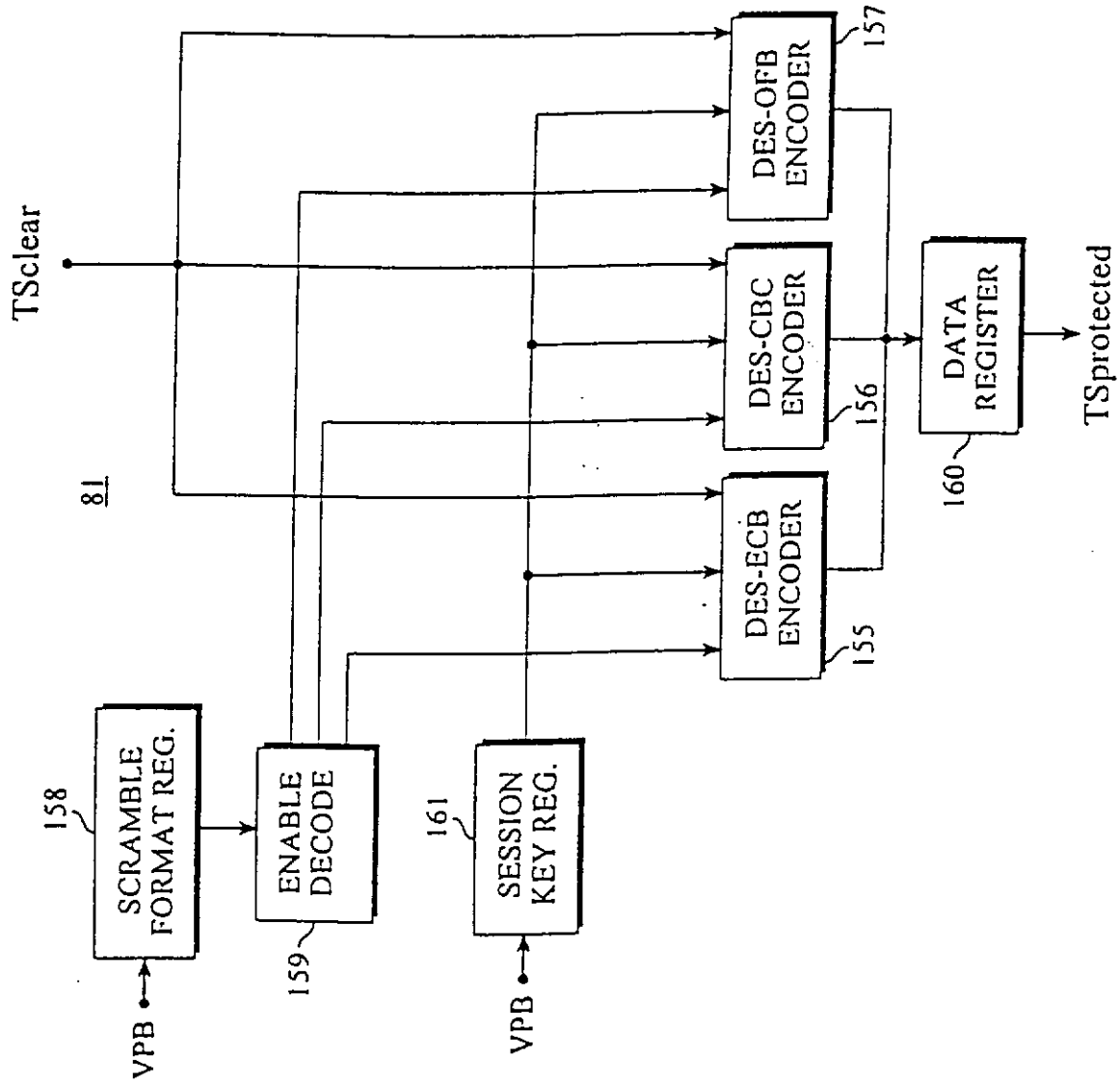

TSclear
81
DES-OFB ENCODER
157
DES-CBC ENCODER
156
DES-ECB ENCODER
155
DATA REGISTER
160
TSprotected
SCRAMBLE FORMAT REG.
158
ENABLE DECODE
159
SESSION KEY REG.
161
VPB
VPB

Fig. 13

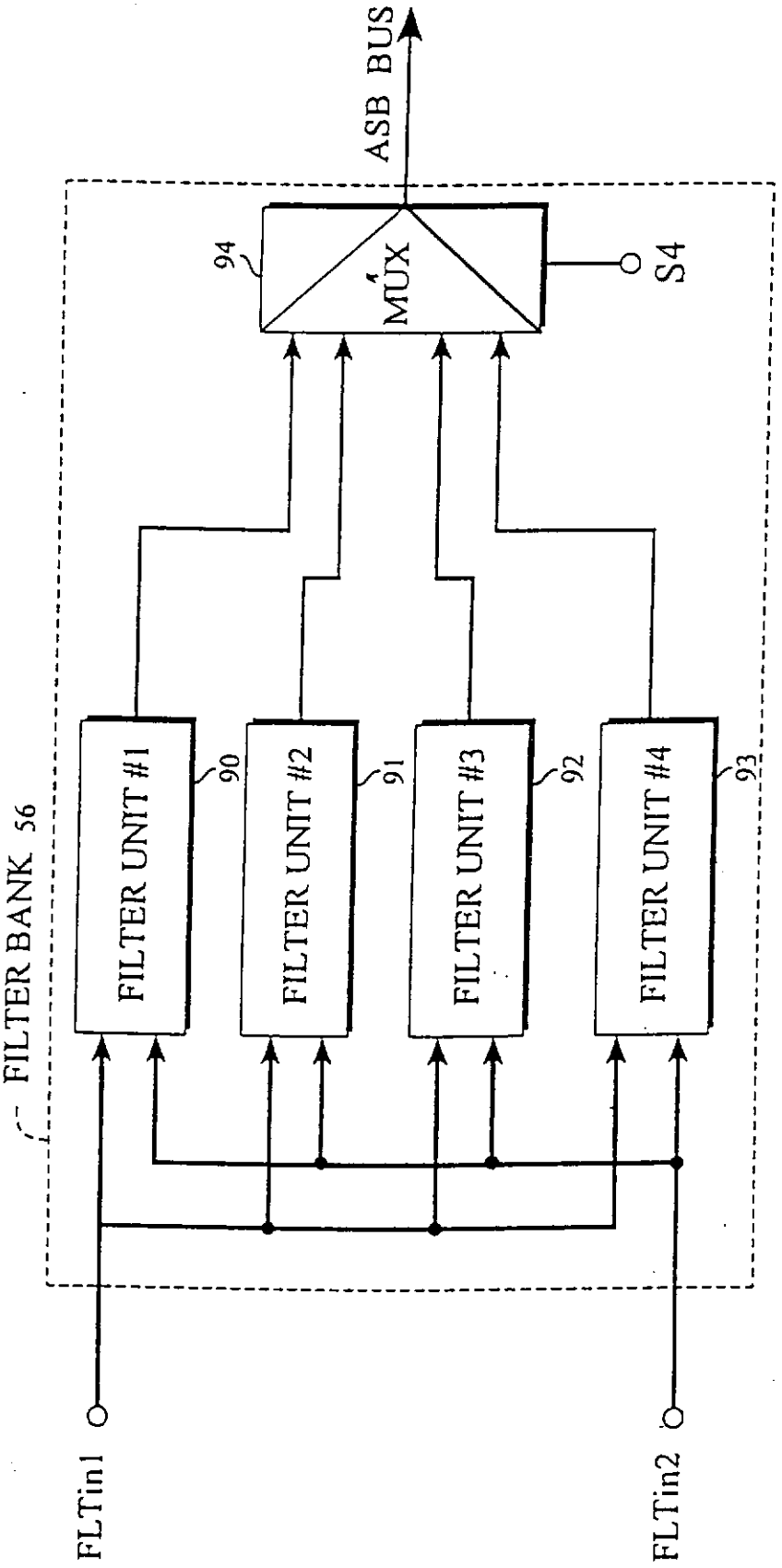

ASB BUS
94
MUX
S4
FILTER BANK 56
FILTER UNIT #1
90
FILTER UNIT #2
91
FILTER UNIT #3
92
FILTER UNIT #4
93
FLTin1
FLTin2

Fig. 14

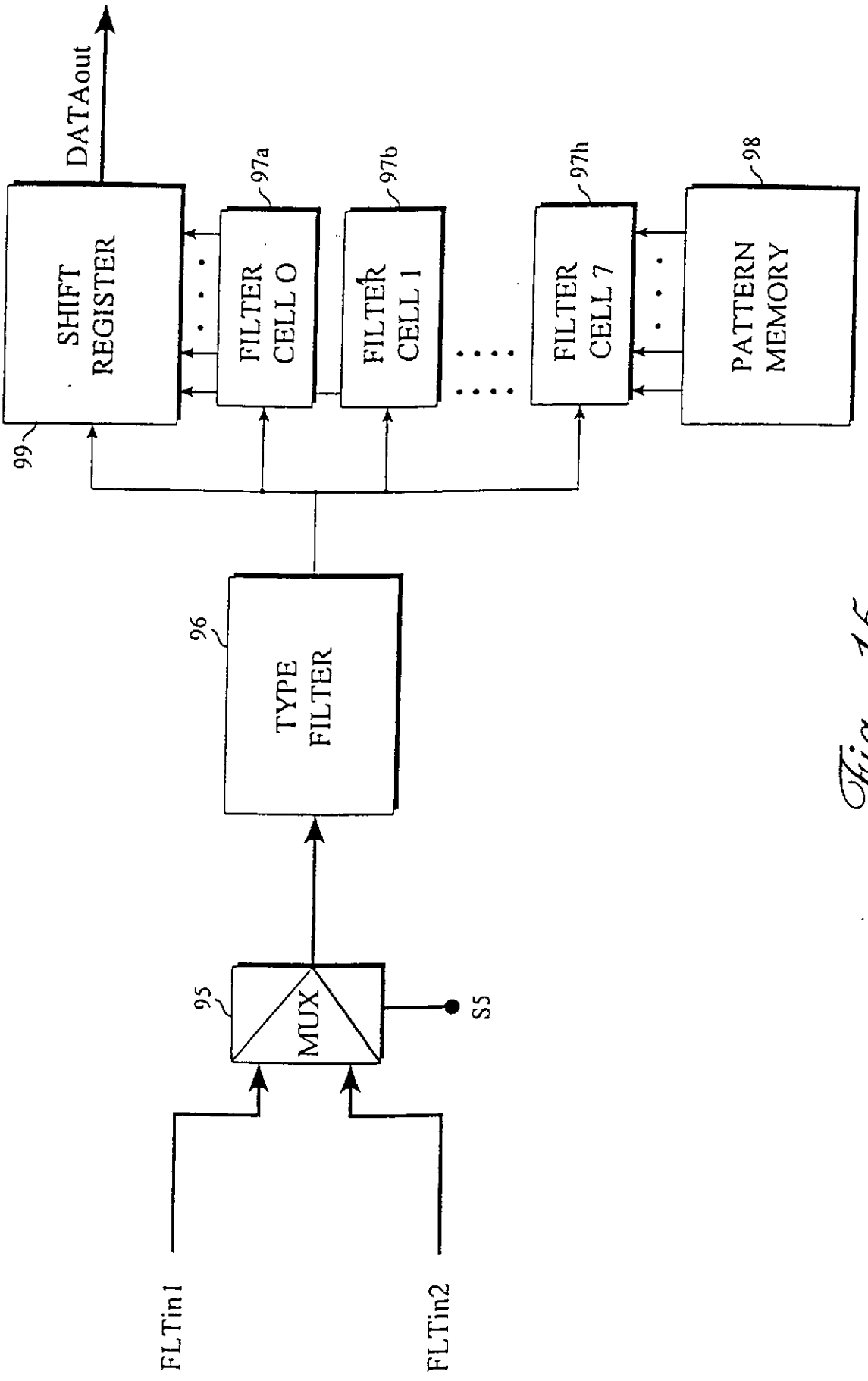

DATAout
SHIFT REGISTER
99
97a
FILTER CELL 0
97b
FILTER CELL 1
97h
FILTER CELL 7
98
PATTERN MEMORY
96
TYPE FILTER
95
MUX
S5
FLTin1
FLTin2

Fig. 15

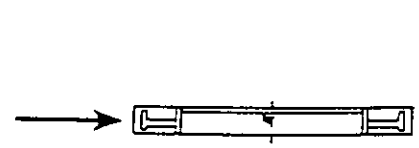


Fig. 16B

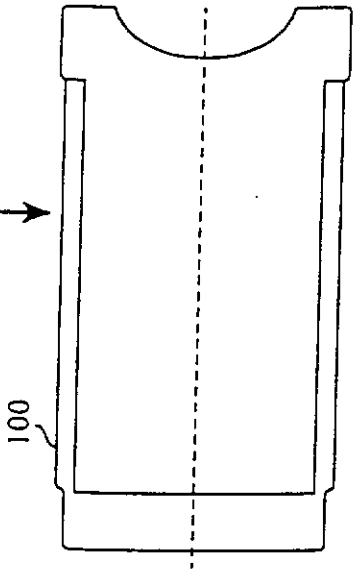


Fig. 16



Fig. 16C

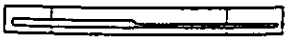


Fig. 16A

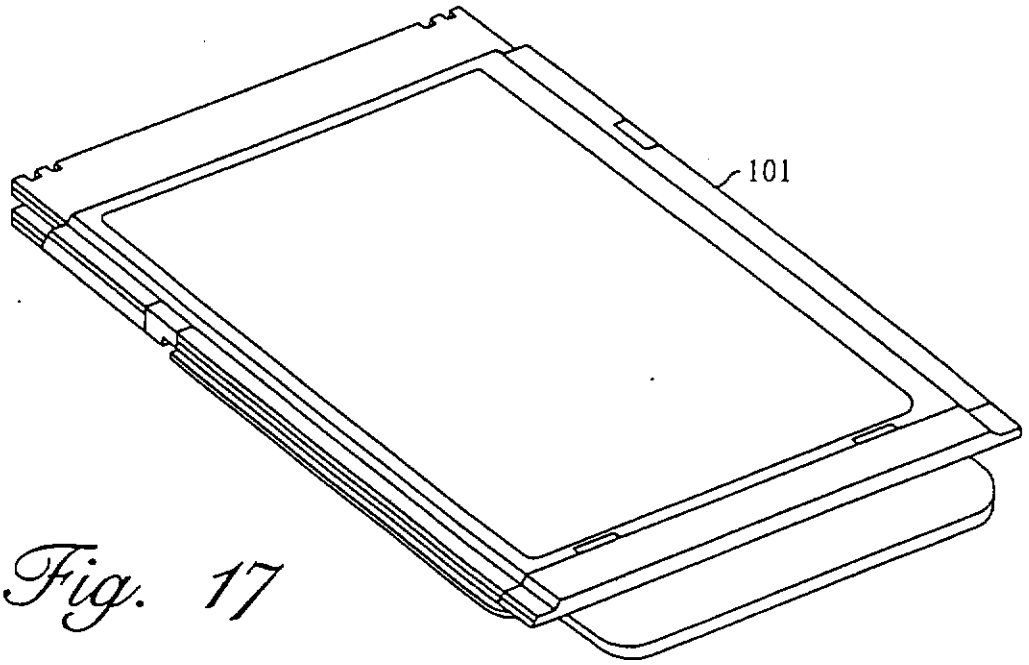


Fig. 17

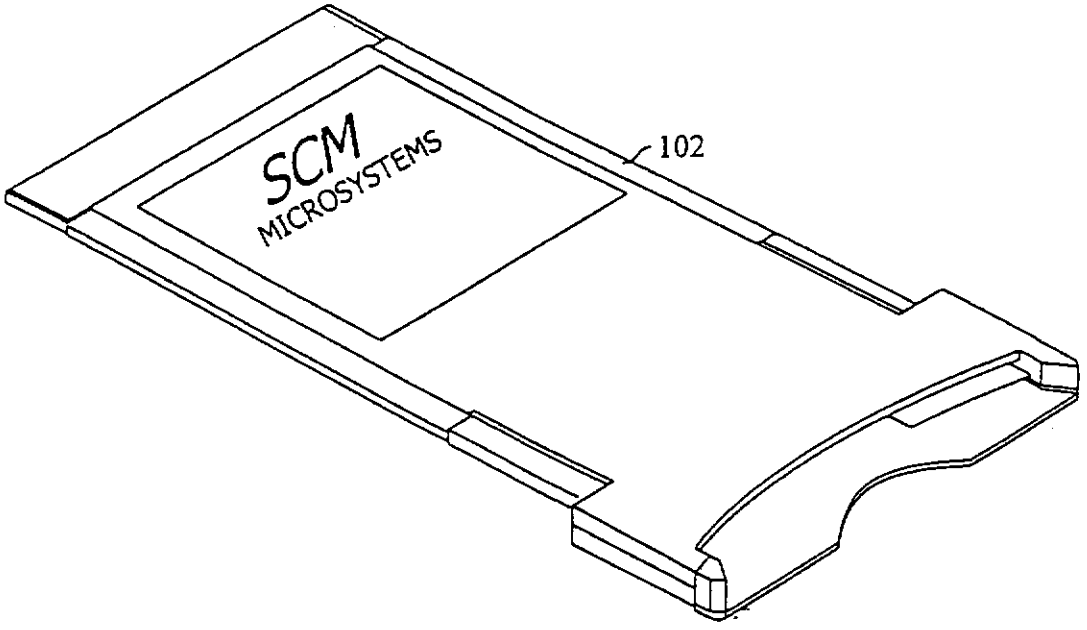


Fig. 18

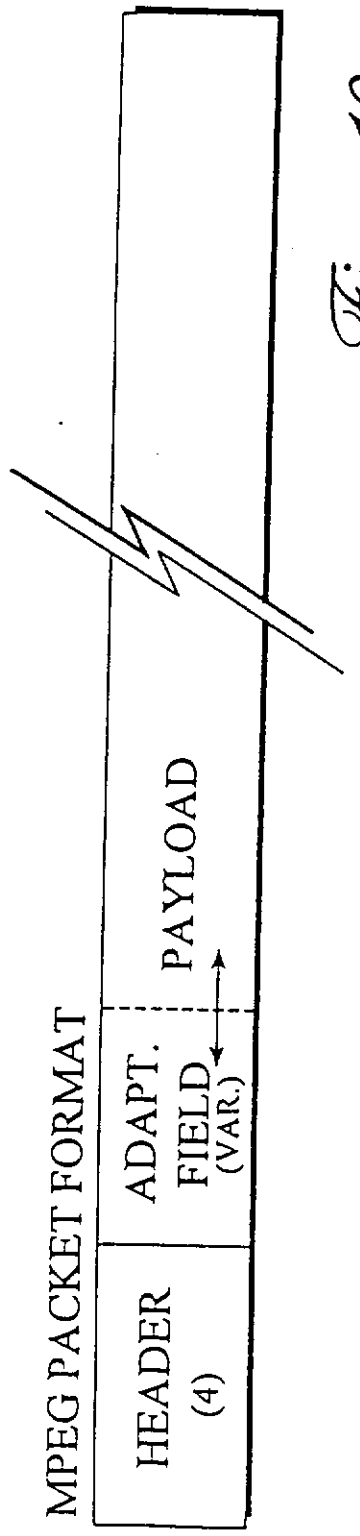


Fig. 19

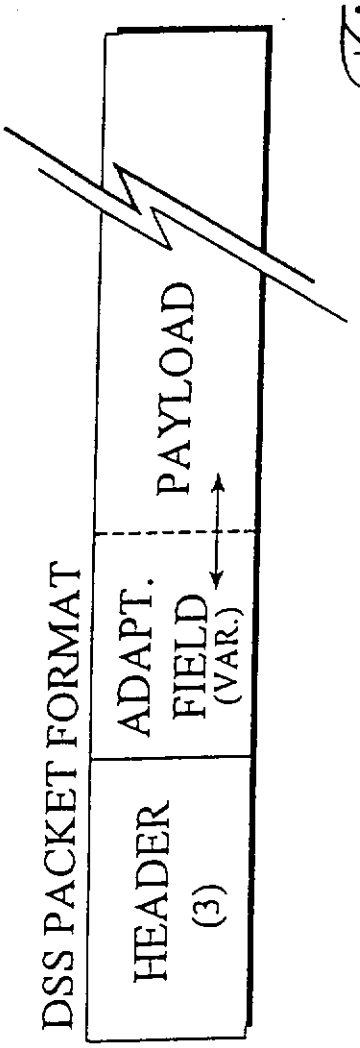


Fig. 20

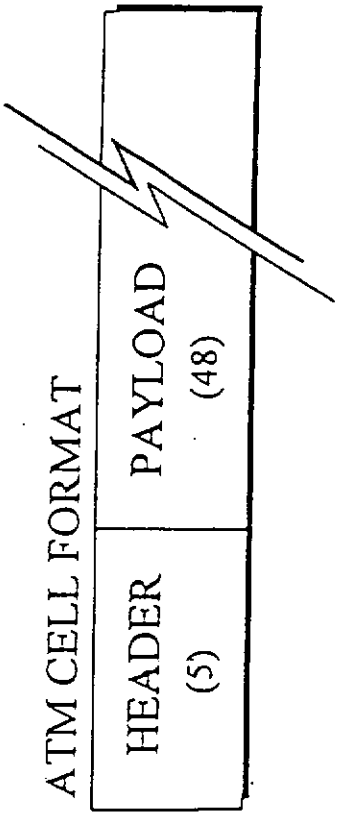


Fig. 21

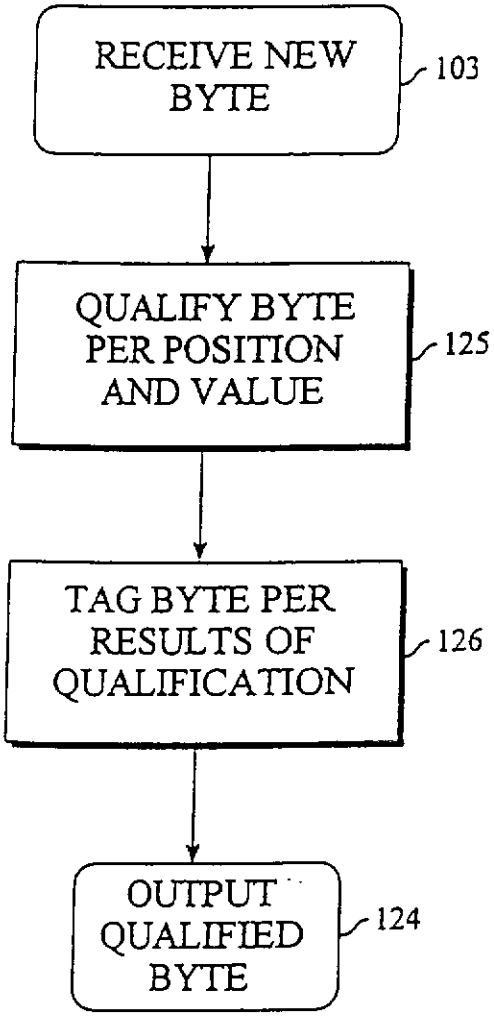

RECEIVE NEW BYTE
103
QUALIFY BYTE PER POSITION AND VALUE
125
TAG BYTE PER RESULTS OF QUALIFICATION
126
OUTPUT QUALIFIED BYTE
124

Fig. 22

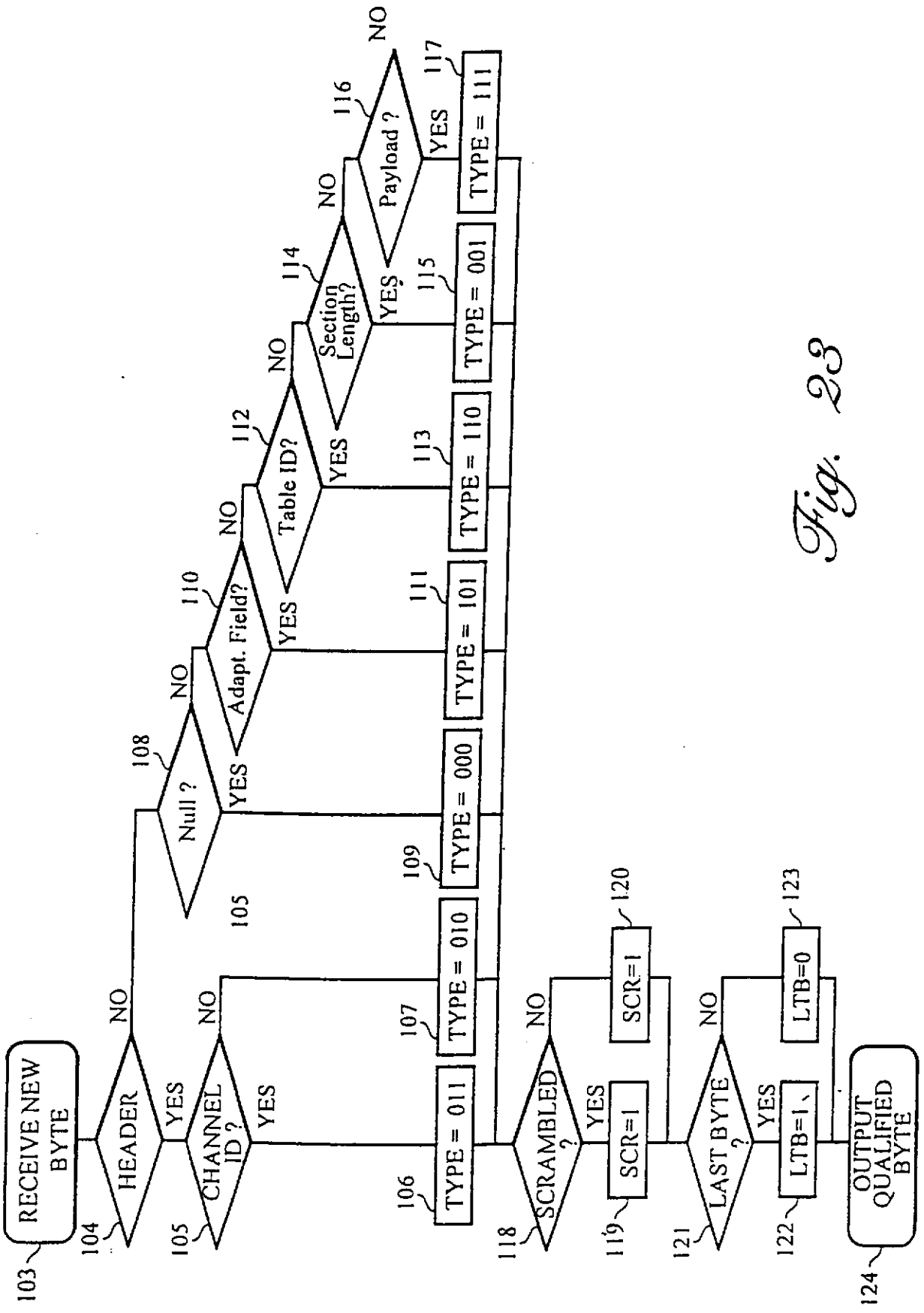

RECEIVE NEW BYTE
103
HEADER
104
NO
YES
CHANNEL ID?
105
NO
YES
TYPE = 011
106
TYPE = 010
107
Null ?
108
NO
YES
TYPE = 000
109
Adapt. Field?
110
NO
YES
TYPE = 101
111
Table ID?
112
NO
YES
TYPE = 110
113
Section Length?
114
NO
YES
TYPE = 001
115
Payload ?
116
NO
YES
TYPE = 111
117
SCRAMBLED ?
118
NO
YES
SCR=1
119
SCR=1
120
LAST BYTE ?
121
NO
YES
LTB=1
122
LTB=0
123
OUTPUT QUALIFIED BYTE
124

Fig. 23

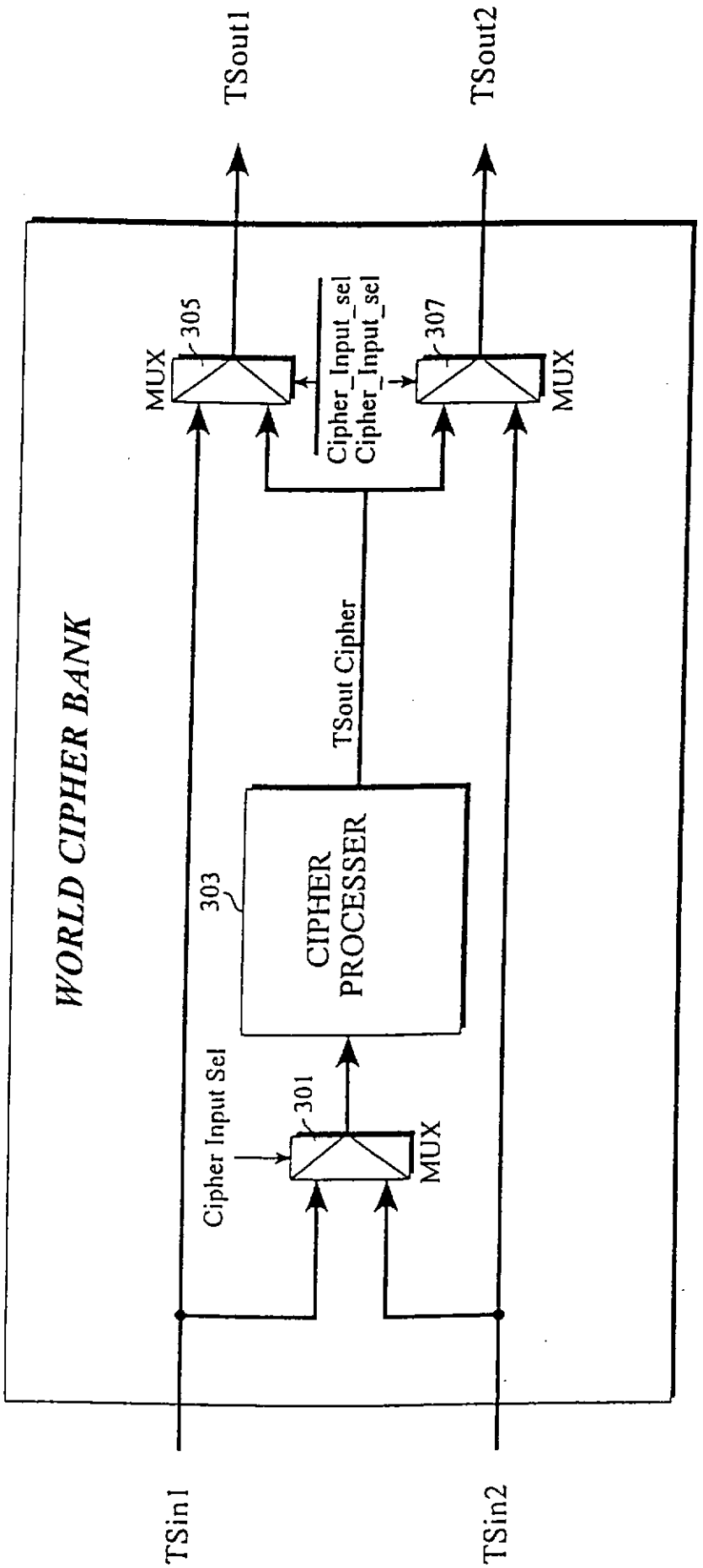

TSout1
TSout2
WORLD CIPHER BANK
MUX
305
Cipher_Input_sel
Cipher_Input_sel
307
MUX
TSout Cipher
303
CIPHER
PROCESSER
Cipher Input Sel
301
MUX
TSin1
TSin2

Fig. 24

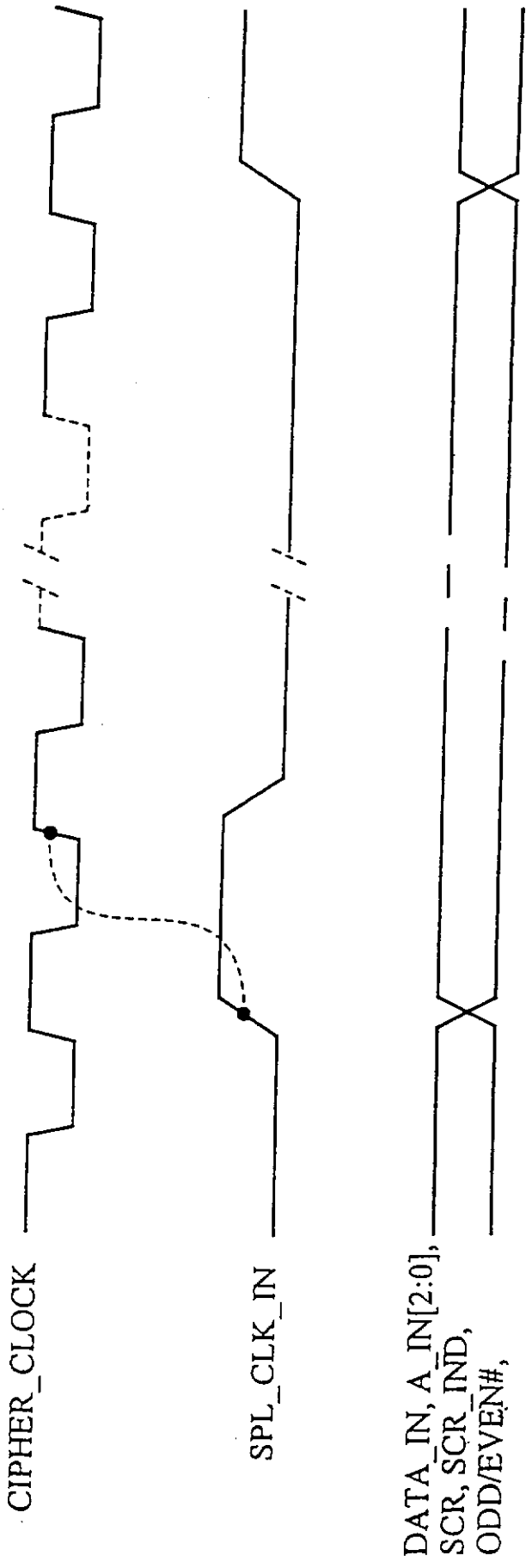


Fig. 25

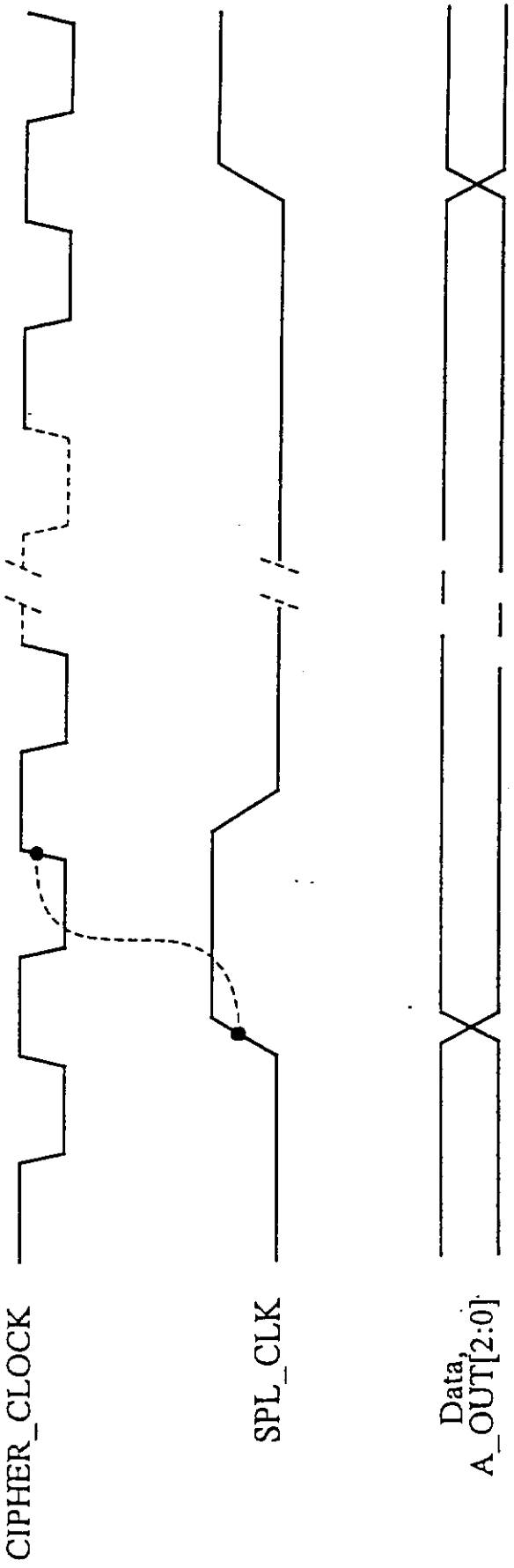


Fig. 26