

**COMPRESSIVE STRESS TRANSFER IN AN INTERLAYER DIELECTRIC OF A  
SEMICONDUCTOR DEVICE BY PROVIDING A BI-LAYER OF SUPERIOR  
ADHESION AND INTERNAL STRESS**

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**ABSTRACT OF THE DISCLOSURE**

The present disclosure provides manufacturing techniques and semiconductor devices (200) in which performance of P-channel transistors (250) may be enhanced on the basis of a stress mechanism that involves the deposition of a dielectric bi-layer (220) system. Contrary  
10 to conventional strategies, an additional pre-treatment may be performed prior to the deposition of an adhesion layer (221) in a plasma-free process atmosphere (204), thereby enabling a reduced thickness of the adhesion layer and a higher internal stress level of the subsequent top layer (222).

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Fig. 2d