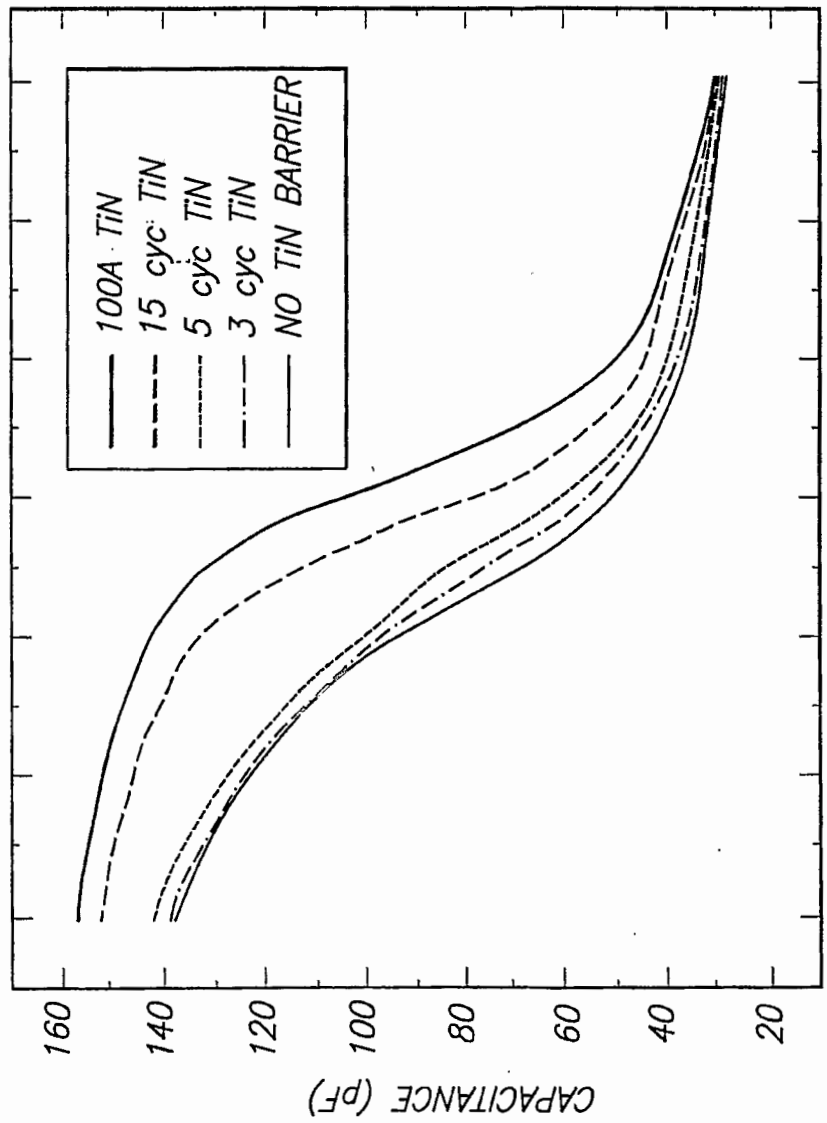

100A TiN
15 cyc TiN
5 cyc TiN
3 cyc TiN
NO TiN BARRIER
CAPACITANCE (pF)
160
140
120
100
80
60
40
20
VOLTAGE (V)
-3
-2
-1
0
1
2
3

FIG 11

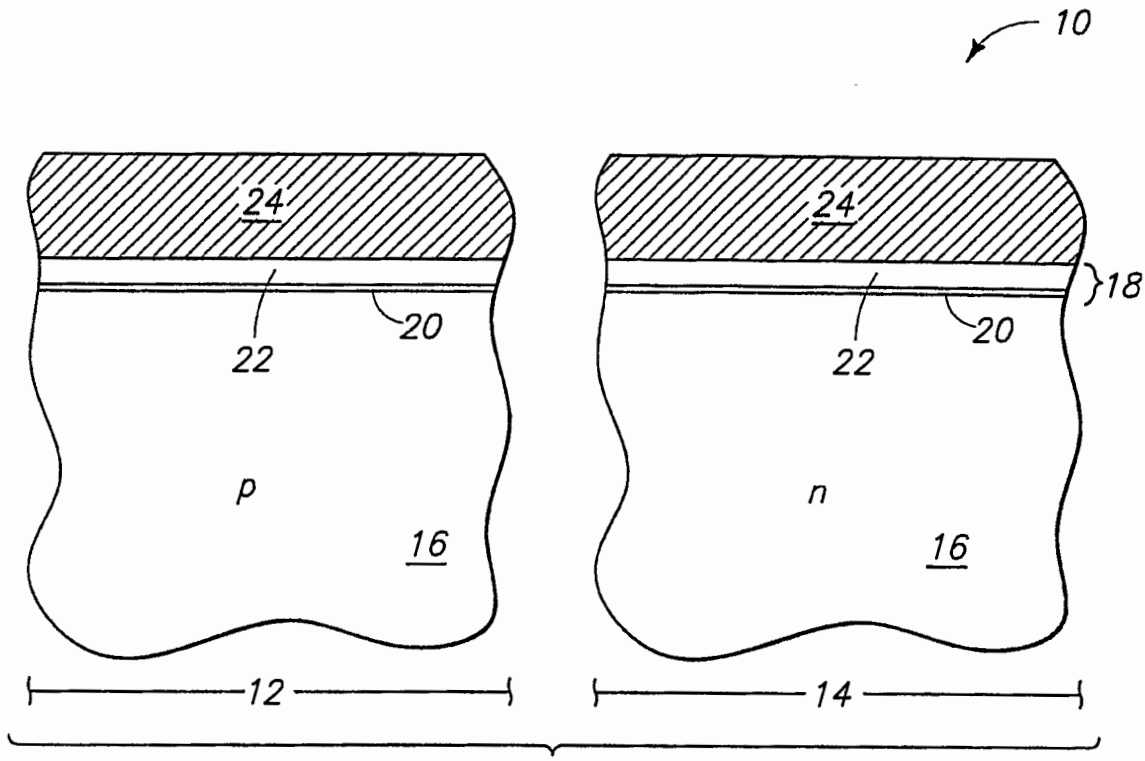

10
24
24
18
22
20
22
20
p
n
16
16
12
14

Fig 2

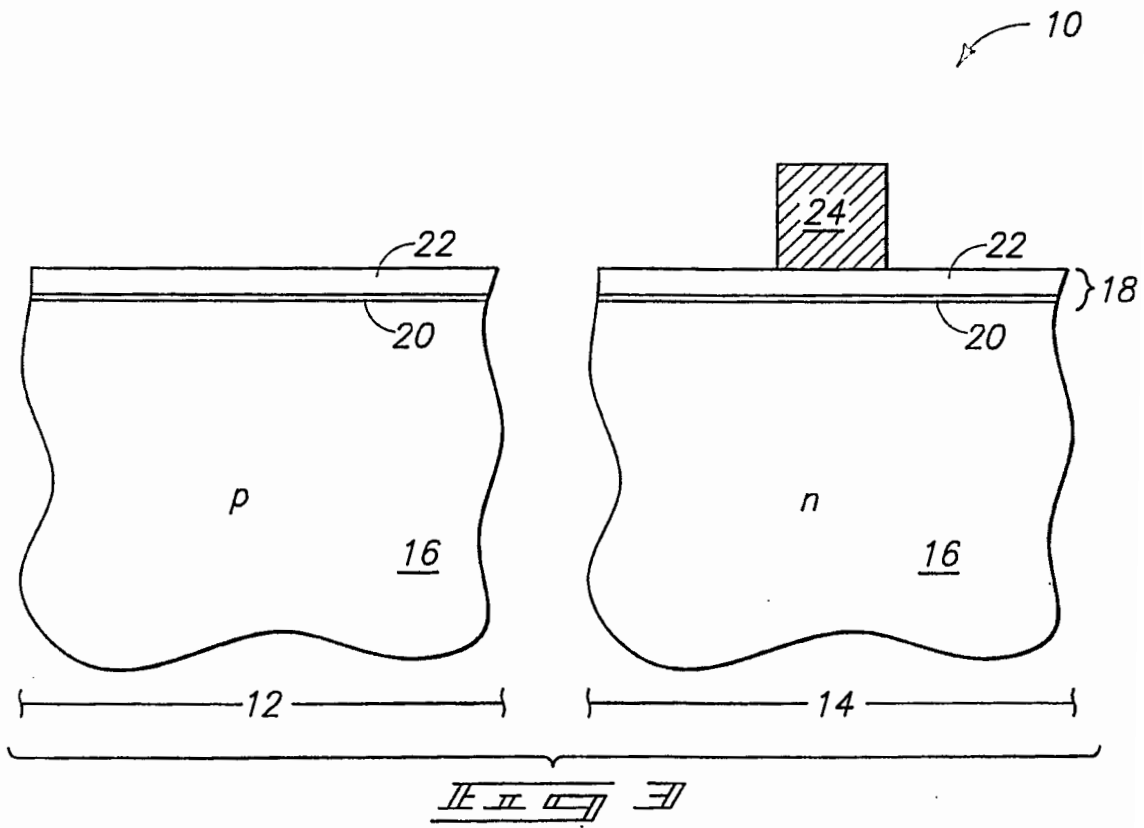

10
24
22
22
18
20
20
p
n
16
16
12
14

Fig 3

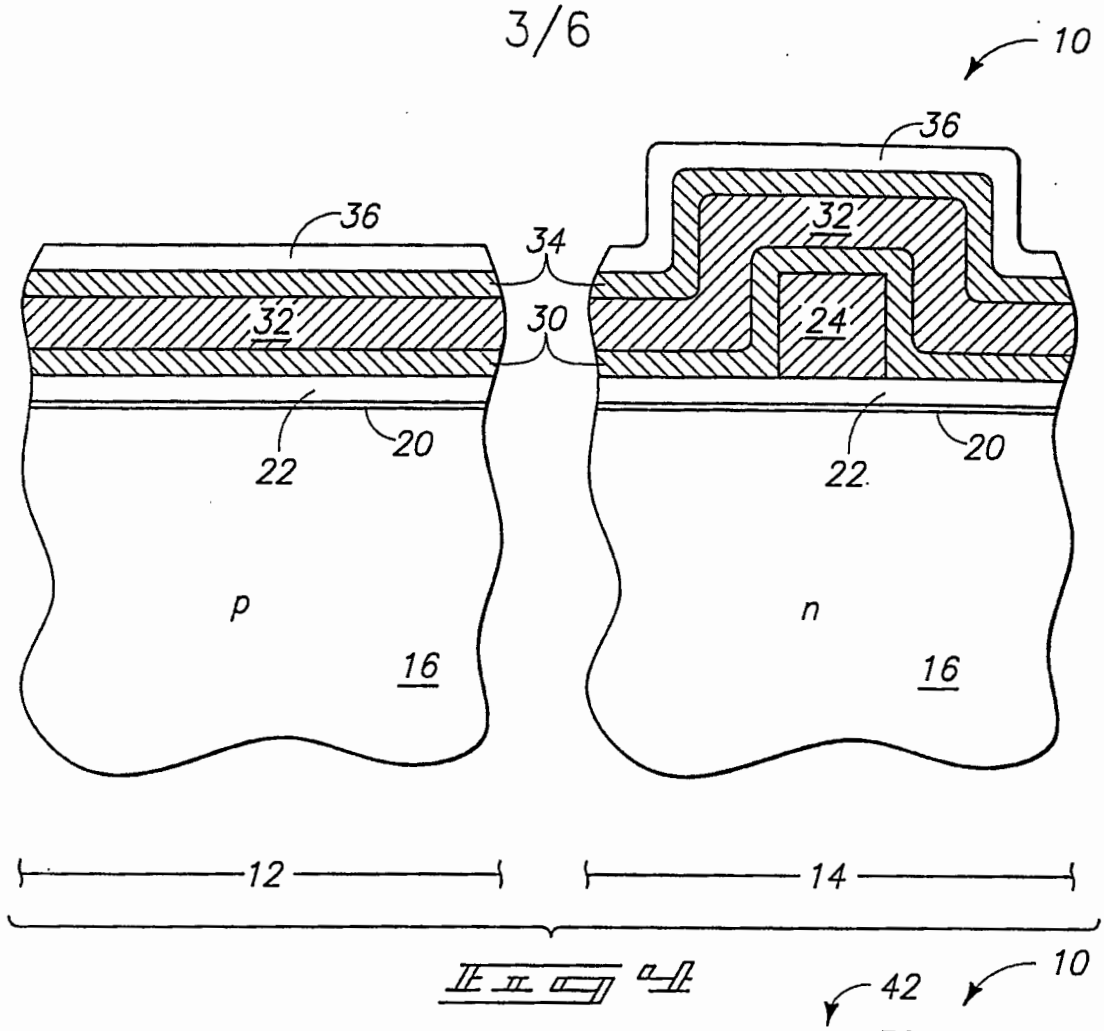

10
36
36
34
32
32
30
24
22
20
22
20
p
n
16
16
12
14

Fig 4

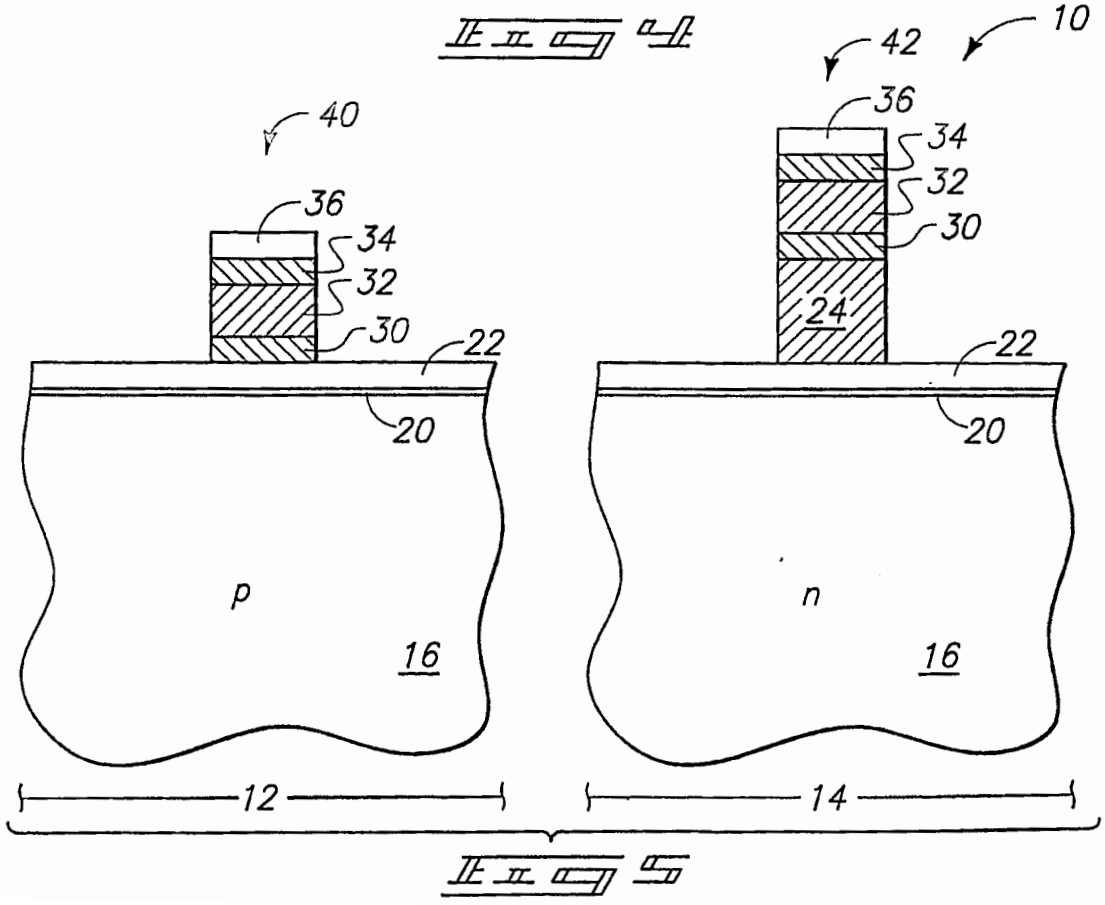

42
10
40
36
36
34
34
32
32
30
30
24
22
22
20
20
p
n
16
16
12
14

Fig 5

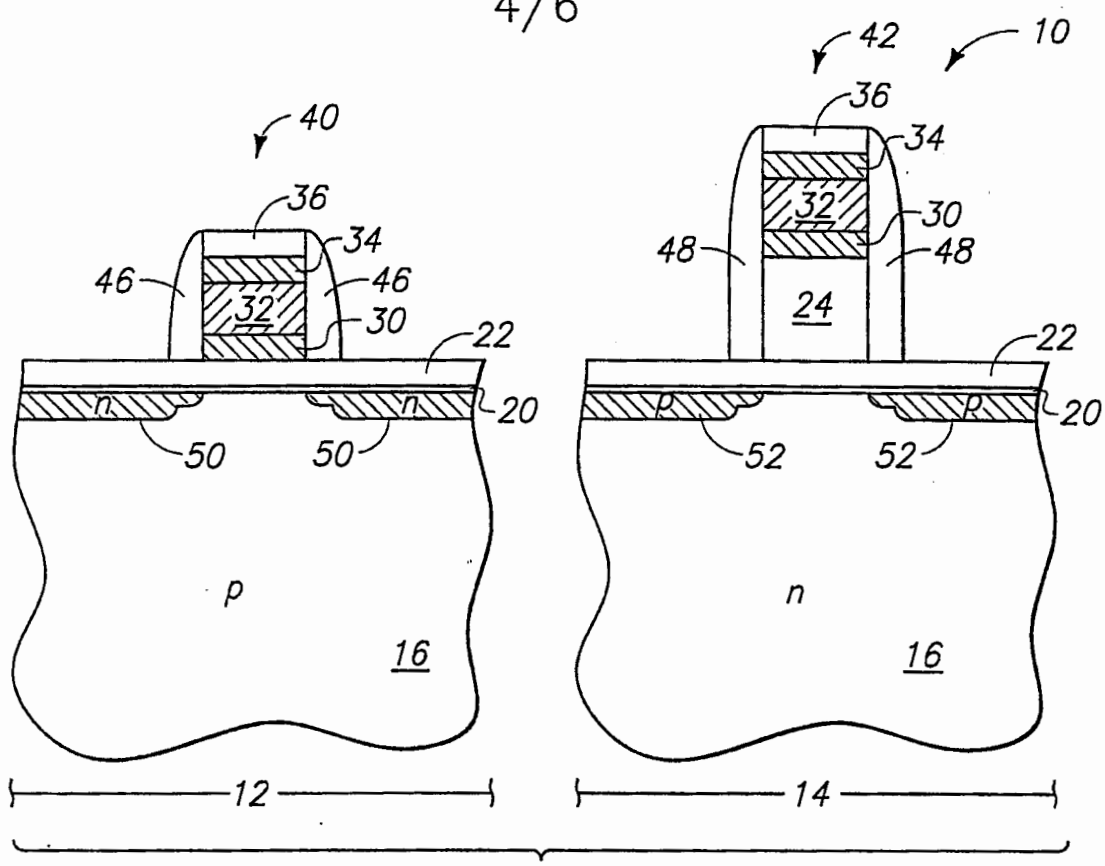

42
10
40
36
34
32
30
46
46
48
48
24
22
22
20
20
n
n
p
p
50
50
52
52
p
n
16
16
12
14

Fig 6

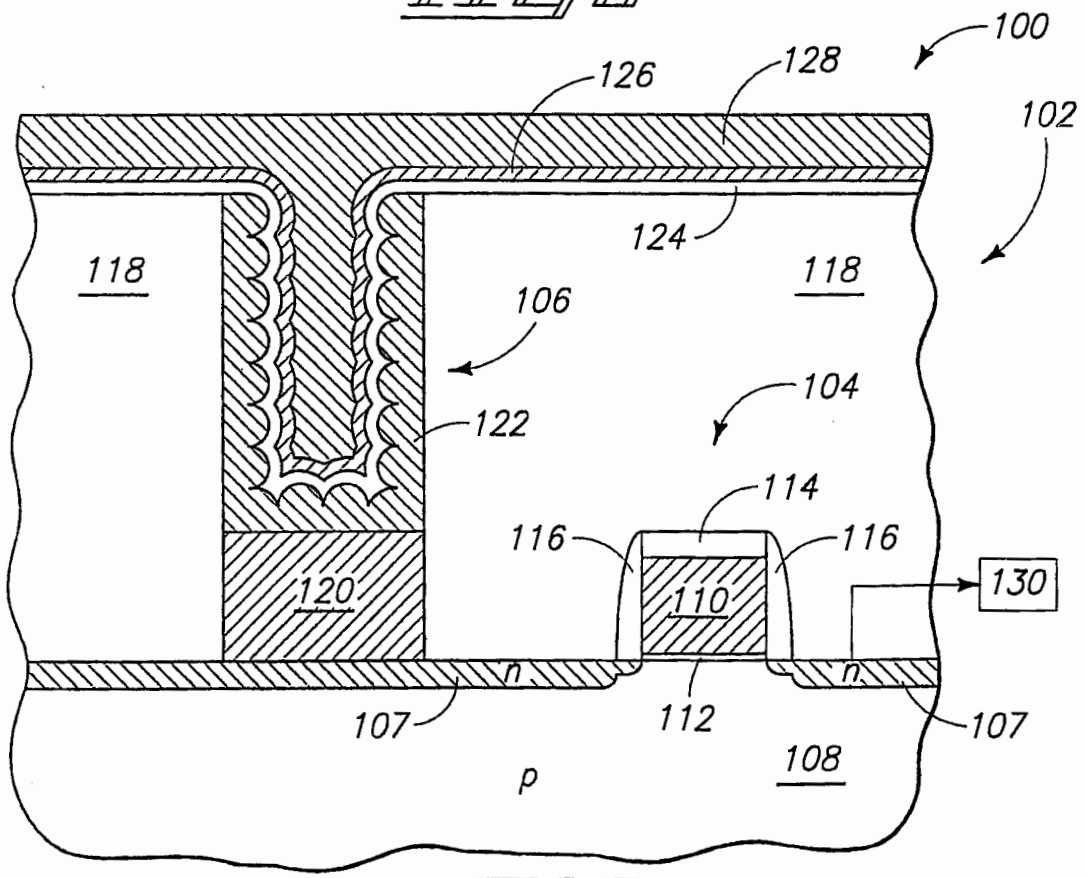

100
126
128
102
124
118
118
106
104
122
114
116
116
120
110
130
n
n
107
112
107
108
p

Fig 7

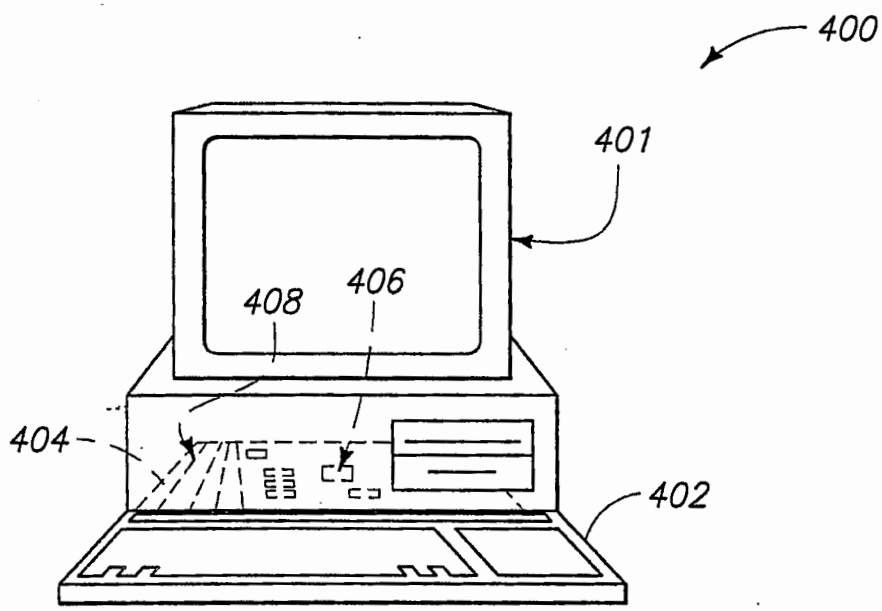


Fig 8

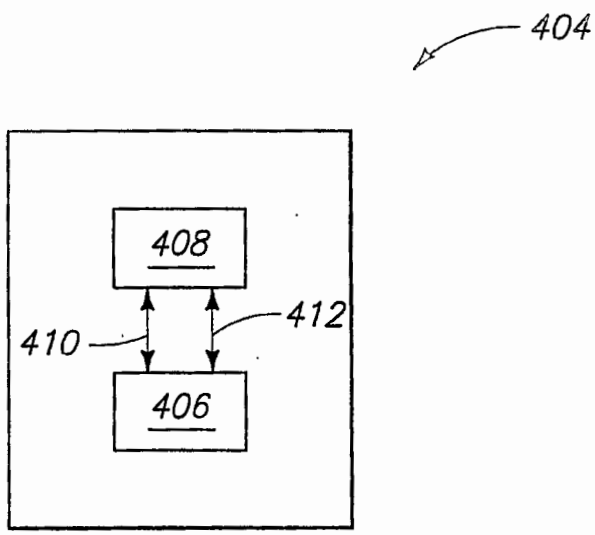


Fig 9

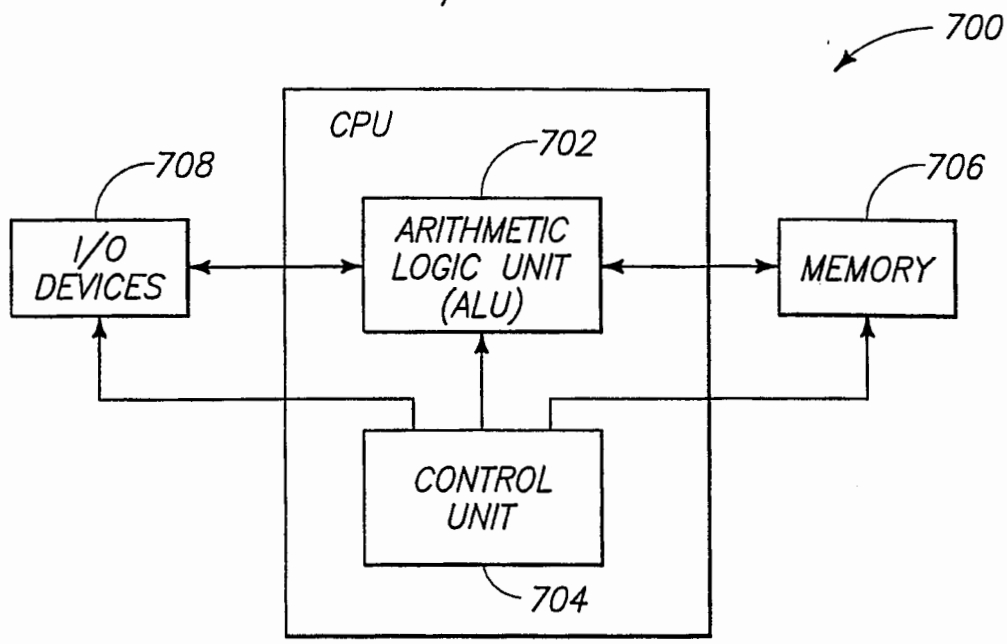

700
CPU
702
708
706
I/O DEVICES
ARITHMETIC LOGIC UNIT (ALU)
MEMORY
CONTROL UNIT
704

Fig. 7

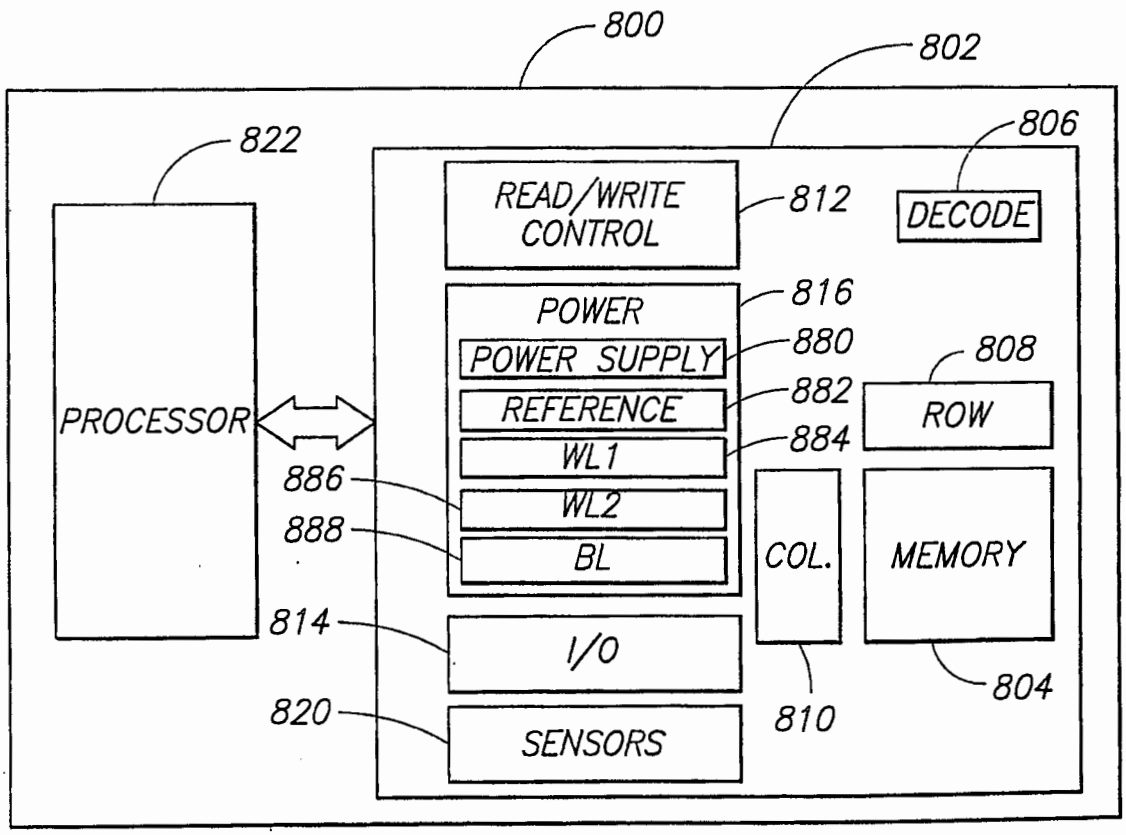

800
802
822
806
READ/WRITE CONTROL
812
DECODE
816
POWER
POWER SUPPLY
880
808
PROCESSOR
REFERENCE
882
ROW
884
WL1
886
WL2
888
BL
COL.
MEMORY
814
I/O
804
820
SENSORS
810

Fig. 11