

A TRELLIS DEMAPPER OF A CONVOLUTIONAL DECODER

ABSTRACT OF THE DISCLOSURE

The trellis demapper, which is capable of demapping 8-PSK and 16, 32, 64, 128 and 256 QAM trellis codes, comprises respective I-channel, Q-channel and remapper RAMs, an 8-PSK demapper logic means and a MUX selects. Each of the RAMs includes a lookup table is selectively programmed for each of the QAM codes. The I-channel RAM and the Q-channel RAM, each of which has a storage capacity of 768 bits, directly forwards their respective outputs through the MUX selects as the trellis demapper output in response to a QAM trellis code which is an even power of 2 (i.e., 16, 64 or 256) being selected. In response to a QAM trellis code which is an odd power of 2 (i.e., 32 or 128) being selected, the respective outputs of the I-channel RAM and the Q-channel RAM are applied as inputs to the remapper RAM, which has a storage capacity of 320 bits, and the output of the remapper RAM is forwarded through the MUX selects as the trellis demapper output. In response to an 8-PSK trellis code being selected, the output of the 8-PSK demapper logic means is forwarded through the MUX selects as the trellis demapper output. This configuration is structurally efficient and requires minimum storage requirements compared to a trellis code demapper employing ROM storage for the 16, 32, 64, 128 and 256 QAM and 8-PSK trellis codes.

FIG. 4