CLAIMS

1. A memory device comprising a plurality of memory elements, the memory elements each comprising:

a first phase-inversion element and a second phase-inversion element which hold data by being connected to each other such that an input terminal of the first phase-inversion element is connected to an output terminal of the second phase-inversion element and an input terminal of the second phase-inversion element is connected to an output terminal of the first phase-inversion element;

a capacitor; and

a transistor which includes an oxide semiconductor in a channel formation region and which is configured to control writing of the data to the capacitor.

2. A memory device comprising a plurality of memory elements, the memory elements each comprising:

a first phase-inversion element;

a second phase-inversion element an input terminal of which is connected to an output terminal of the first phase-inversion element;

a first switching element which is configured to control input of a signal including data to an input terminal of the first phase-inversion element;

a second switching element which is configured to control connection between the input terminal of the first phase-inversion element and an output terminal of the second phase-inversion element;

a capacitor; and

a transistor which includes an oxide semiconductor in a channel formation region and which is configured to control writing of the data to the capacitor.

3. A memory device comprising a plurality of memory elements, the memory elements each comprising:

a first phase-inversion element;

a second phase-inversion element an input terminal of which is connected to an output terminal of the first phase-inversion element;

a first switching element which is configured to control input of a signal including data to an input terminal of the first phase-inversion element;

a second switching element which is configured to control connection between the input terminal of the first phase-inversion element and an output terminal of the second phase-inversion element;

a capacitor; and

a transistor which includes an oxide semiconductor in a channel formation region and which is configured to control connection between the input terminal of the first phase-inversion element and the capacitor.

4. A memory device comprising a plurality of memory elements, the memory elements each comprising:

a first phase-inversion element;

a second phase-inversion element an input terminal of which is connected to an output terminal of the first phase-inversion element;

a first switching element which is configured to control input of a signal including data to an input terminal of the first phase-inversion element;

a second switching element which is configured to control connection between the input terminal of the first phase-inversion element and an output terminal of the second phase-inversion element;

a third switching element which is configured to control output of a potential of the output terminal of the first phase-inversion element;

a capacitor;

a transistor which includes an oxide semiconductor in a channel formation region and which is configured to control writing of the data to the capacitor;

a third phase-inversion element an input terminal of which is supplied with a potential including the data written in the capacitor; and

a fourth switching element which is configured to control output of a potential of an output terminal of the third phase-inversion element.

5. A memory device comprising a plurality of memory elements, the memory elements each comprising:

a first phase-inversion element;

a second phase-inversion element an input terminal of which is connected to an output terminal of the first phase-inversion element;

a first switching element which is configured to control connection between an input terminal of the first phase-inversion element and a node to which a signal including data is input;

a second switching element which is configured to control connection between the input terminal of the first phase-inversion element and an output terminal of the second phase-inversion element;

a third switching element which is configured to control output of a potential of the output terminal of the first phase-inversion element;

a capacitor;

a transistor which includes an oxide semiconductor in a channel formation region and which is configured to control connection between the node and the capacitor;

a third phase-inversion element an input terminal of which is supplied with a potential including the data written in the capacitor; and

a fourth switching element which is configured to control output of a potential of an output terminal of the third phase-inversion element.

6. The memory device according to any one of claims 1 to 5, wherein an OFF-state current density of the transistor is less than or equal to 100 zA/μm.

7. A memory device comprising a plurality of memory elements, the memory elements each comprising:

a first phase-inversion element;

a second phase-inversion element an input terminal of which is connected to an output terminal of the first phase-inversion element;

a first switching element which is configured to control input of a signal including data to an input terminal of the first phase-inversion element;

a second switching element which is configured to control connection between the input terminal of the first phase-inversion element and an output terminal of the

second phase-inversion element;

a first capacitor;

a first transistor which includes an oxide semiconductor in a channel formation region and which is configured to control writing of the data to the first capacitor;

a second capacitor; and

a second transistor which includes an oxide semiconductor in a channel formation region and which is configured to control writing of the data to the second capacitor.

8. A memory device comprising a plurality of memory elements, the memory elements each comprising:

a first phase-inversion element;

a second phase-inversion element an input terminal of which is connected to an output terminal of the first phase-inversion element;

a first switching element which is configured to control input of a signal including data to an input terminal of the first phase-inversion element;

a second switching element which is configured to control connection between the input terminal of the first phase-inversion element and an output terminal of the second phase-inversion element;

a first capacitor;

a first transistor which includes an oxide semiconductor in a channel formation region and which is configured to control connection between the input terminal of the first phase-inversion element and the first capacitor;

a second capacitor; and

a second transistor which includes an oxide semiconductor in a channel formation region and which is configured to control connection between the output terminal of the first phase-inversion element and the second capacitor.

9. The memory device according to claim 7 or claim 8, wherein an OFF-state current density of the first transistor or the second transistor is less than or equal to 100 zA/μm.

10. The memory device according to any one of claims 1, 2, 3, 7, and 8, wherein each of the first and second phase-inversion elements is one selected from the group of an inverter and a clocked inverter.

11. The memory device according to any one of claims 1, 2, 3, 4, 5, 7, and 8, wherein the oxide semiconductor is an In-Ga-Zn-O-based oxide semiconductor.

12. The memory device according to any one of claim 1, 2, 3, 4, 5, 7, and 8, wherein an hydrogen concentration in the channel formation region is lower than or equal to 5×10^{19} /cm^3.

13. A semiconductor device which is an LSI comprising a CPU, a DSP, or a microcontroller comprising the memory device according to any one of claims 1, 2, 3, 4, 5, 7, and 8.

14. An electric device including one selected from the group consisting of a game machine, an image reproducing device, and a personal computer each comprising the memory device according to any one of claims 1, 2, 3, 4, 6, 7, and 8.

15. The memory device according to claim 4 or claim 5, wherein each of the first, second and third phase-inversion elements is one selected from the group of an inverter and a clocked inverter.

CLAIMS

1. A semiconductor device comprising:

a first logic element;

a second logic element;

a third logic element;

a first transistor comprising a first terminal, a second terminal, and a gate;

a second transistor comprising a first terminal, a second terminal, and a gate;

a third transistor comprising a first terminal, a second terminal, and a gate;

a fourth transistor comprising a first terminal, a second terminal, and a gate;

a fifth transistor comprising a first terminal, a second terminal, and a gate; and

a capacitor,

wherein:

an input terminal of the first logic element is electrically connected to the second terminal of the first transistor and the first terminal of the second transistor,

an output terminal of the first logic element is electrically connected to an input terminal of the second logic element and the first terminal of the third transistor,

an output terminal of the second logic element is electrically connected to the second terminal of the second transistor,

the second terminal of the third transistor is electrically connected to the first terminal of the fifth transistor,

the second terminal of the fifth transistor is electrically connected to an output terminal of the third logic element,

an input terminal of the third logic element is electrically connected to the second terminal of the fourth transistor and the capacitor,

the first terminal of the fourth transistor is electrically connected to the first terminal of the first transistor, and

a channel formation region of the fourth transistor comprises an oxide semiconductor comprising at least indium and zinc.

2. The semiconductor device according to claim 1, wherein each of the first to third logic elements is any of an inverter and a clocked inverter.

3. The semiconductor device according to claim 1, wherein an off-state current of the fourth transistor is lower than or equal to 100 zA/μm.

4. The semiconductor device according to claim 1, wherein the oxide semiconductor further comprises gallium.

5. A semiconductor device which is an LSI comprising a CPU, a DSP, or a microcontroller comprising the semiconductor device according to claim 1.

6. An electronic device comprising a CPU comprising the semiconductor device according to claim 1, wherein the electronic device is one selected from the group consisting of a game machine, an image reproducing device, and a personal computer.

7. A semiconductor device comprising:
a first logic element;
a second logic element;
a third logic element;
a first transistor comprising a first terminal, a second terminal, and a gate;
a second transistor comprising a first terminal, a second terminal, and a gate;
a third transistor comprising a first terminal, a second terminal, and a gate;
a fourth transistor comprising a first terminal, a second terminal, and a gate;
a fifth transistor comprising a first terminal, a second terminal, and a gate; and
a capacitor,
wherein:
an input terminal of the first logic element is electrically connected to the second

terminal of the first transistor and the first terminal of the second transistor,

an output terminal of the first logic element is electrically connected to an input terminal of the second logic element and the first terminal of the third transistor,

an output terminal of the second logic element is electrically connected to the second terminal of the second transistor,

the second terminal of the third transistor is electrically connected to the first terminal of the fifth transistor,

the second terminal of the fifth transistor is electrically connected to an output terminal of the third logic element,

an input terminal of the third logic element is electrically connected to the second terminal of the fourth transistor and the capacitor,

the first terminal of the fourth transistor is electrically connected to the first terminal of the first transistor, and

a channel formation region of the fourth transistor comprises an oxide semiconductor comprising at least indium and zinc, and

a hydrogen concentration in the channel formation region is lower than or equal to 5 x 10^{19} /cm^3.

8. The semiconductor device according to claim 7, wherein each of the first to third logic elements is any of an inverter and a clocked inverter.

9. The semiconductor device according to claim 7, wherein an off-state current of the fourth transistor is lower than or equal to 100 zA/μm.

10. The semiconductor device according to claim 7, wherein the oxide semiconductor further comprises gallium.

11. A semiconductor device which is an LSI comprising a CPU, a DSP, or a microcontroller comprising the semiconductor device according to claim 7.

12. An electronic device comprising a CPU comprising the semiconductor device according to claim 7, wherein the electronic device is one selected from the group consisting of a game machine, an image reproducing device, and a personal computer.

13. A semiconductor device comprising:

a first logic element;

a second logic element;

a third logic element;

a first transistor comprising a first terminal, a second terminal, and a gate;

a second transistor comprising a first terminal, a second terminal, and a gate;

a third transistor comprising a first terminal, a second terminal, and a gate;

a fourth transistor comprising a first terminal, a second terminal, and a gate;

a fifth transistor comprising a first terminal, a second terminal, and a gate; and

a capacitor,

wherein:

an input terminal of the first logic element is electrically connected to the second terminal of the first transistor and the first terminal of the second transistor,

an output terminal of the first logic element is electrically connected to an input terminal of the second logic element and the first terminal of the third transistor,

an output terminal of the second logic element is electrically connected to the second terminal of the second transistor,

the second terminal of the third transistor is electrically connected to the first terminal of the fifth transistor,

the second terminal of the fifth transistor is electrically connected to an output terminal of the third logic element,

an input terminal of the third logic element is electrically connected to the second terminal of the fourth transistor and the capacitor,

the first terminal of the fourth transistor is electrically connected to the first terminal

of the first transistor,

a channel formation region of the fourth transistor comprises an oxide semiconductor comprising at least indium and zinc, and

the channel formation region of the fourth transistor further comprises crystals which are c-axis-oriented in a direction generally perpendicular to a surface of the oxide semiconductor.

14. The semiconductor device according to claim 13, wherein each of the first to third logic elements is any of an inverter and a clocked inverter.

15. The semiconductor device according to claim 13, wherein an off-state current of the fourth transistor is lower than or equal to 100 zA/μm.

16. The semiconductor device according to claim 13, wherein the oxide semiconductor further comprises gallium.

17. A semiconductor device which is an LSI comprising a CPU, a DSP, or a microcontroller comprising the semiconductor device according to claim 13.

18. An electronic device comprising a CPU comprising the semiconductor device according to claim 13, wherein the electronic device is one selected from the group consisting of a game machine, an image reproducing device, and a personal computer.