

CLAIMS:

1. An integrated circuit device (100) comprising:
 - a semiconductor substrate (101) having a resistivity of at least 100 $\Omega\cdot\text{cm}$;
 - an electrically insulating layer (102) that contacts the semiconductor substrate, the electrically insulating layer being susceptible of inducing in the
 - 5 semiconductor substrate a parasitic surface conduction layer that interfaces with the electrically insulating layer; and
 - an electrical circuit (103) located on the electrically insulating layer, wherein the integrated circuit device comprises a depletion-inducing junction (108, 109) of which at least a portion is comprised in the semiconductor substrate,
 - 10 the depletion-inducing junction being adapted to autonomously induce in the semiconductor substrate a depleted zone (301) that interfaces with a section of the electrically insulating layer that lies in-between two sections (104, 105) of the electrical circuit.
- 15 2. An integrated circuit device according to claim 1, wherein the depletion-inducing junction (108, 109) comprises a doped region (108) in the semiconductor substrate (101) near the electrically insulating layer (102) the doped region having polarity that is opposite to a polarity of free charge carriers in an adjacent region where a bulk section of the semiconductor substrate interfaces with the electrically insulating layer.
- 20 3. An integrated circuit device according to claim 2, wherein the depletion-inducing junction (108, 109) comprises another doped region (109) in the semiconductor substrate (101) near the electrically insulating layer (102), the one and the other doped region interfacing with each other and having opposite polarities.
- 25 4. An integrated circuit device according to claim 1, wherein the depletion-inducing junction comprises an electrical conductor (1204) that traverses the electrically

insulating layer (1202) and that interfaces with the semiconductor substrate (1201) thereby forming a Schottky contact.

5. An integrated circuit device according to any of claims 1 to 4, comprising a set of electrical contacts (701) through which a biasing voltage can be applied to the depletion-inducing junction (108, 109).

6. An integrated circuit device according to any of claims 1 to 5, wherein the depletion-inducing junction (108, 109) is disposed a loop-like manner surrounding at least one of the two sections of the electrical circuit.

7. An integrated circuit device according to any of claims 1 and 6, wherein the depletion-inducing junction (108, 109) is part of a plurality of depletion-inducing junctions (107) adapted to autonomously induce in the semiconductor substrate (101) a plurality of depleted zones that interface with the section of the electrically insulating layer (102) that lies in-between the two sections of the electrical circuit..

8. An integrated circuit device according to claim 7, wherein the depletion-inducing junctions are disposed in an array-like manner.

9. An integrated circuit device according to claim 7, wherein the depletion-inducing junctions are disposed in a checkerboard-like manner.

10. A semiconductor wafer adapted for manufacturing an integrated circuit device (100) according to any of claims 1 to 9, the semiconductor wafer comprising:

- a semiconductor substrate having a resistivity of at least 100 Ω .cm;
- an electrically insulating layer that contacts the semiconductor substrate, the electrically insulating layer being susceptible of inducing in the semiconductor substrate a parasitic surface conduction layer that interfaces with the electrically insulating layer; and
- a semiconductor layer located on the electrically insulating layer in which the electrical circuit can be formed,

wherein the semiconductor wafer comprises a depletion-inducing junction of which at least a portion is comprised in the semiconductor substrate, the depletion-

inducing junction being adapted to autonomously induce in the semiconductor substrate a depleted zone that interfaces with a section of the electrically insulating layer.

11. A method of manufacturing an integrated circuit device (100) according to
5 any of claims 1 to 9, comprising the step of forming a depletion-inducing junction (108, 109) at least partially in a semiconductor substrate having a resistivity of at least 100 Ω .cm, the depletion-inducing junction being adapted to autonomously induce in the semiconductor substrate a depleted zone (301) that interfaces with a section of an electrically insulating layer susceptible of inducing in the semiconductor substrate a
10 parasitic surface conduction layer that interfaces with the electrically insulating layer.
12. A method of manufacturing according to claim 11, wherein the depletion-inducing junction is formed using a processing step that is also used to form the electrical circuit.
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13. A method of manufacturing according to claim 11, wherein the depletion-inducing junction is at least partially formed using at least one of the following techniques: implantation and diffusion.