Claims

1. A photonic integrated chip, PIC, configured for alignment and attachment of a laser diode in a predetermined position in which light from the laser diode is aligned with an input of the PIC;

wherein the photonic chip comprises an asymmetric alignment assembly for receiving and aligning the laser diode in the predetermined position; and

wherein the input comprises a coupler for receiving a laser beam from the laser diode in use.

2. The photonic integrated chip according to claim 1, wherein the asymmetric alignment arrangement comprises a plurality of alignment keys configured to align the attachment of the laser diode in the predetermined position.

3. The photonic integrated chip according to claim 2, wherein at least one pair of alignment keys are asymmetric relative to one another.

4. The photonic integrated chip according to claim 3, wherein the pair of alignment keys are elongate and run along a direction substantially parallel to the laser beam in use.

5 The photonic integrated chip according to claim 4, wherein the pair of alignment keys include a gap between them defining a channel through which the laser waveguide can be aligned.

6. The photonic integrated chip according to claim 5, wherein the gap includes a central region having a uniform profile and two sections at either end, each having a respective first irregular profile and second irregular profile; and

wherein the first irregular profile of one of the pair is juxtaposed to the second irregular profile of the other of the pair.

7. The photonic integrated chip according to any preceding claim, wherein the alignment assembly includes a second alignment element.

8. The photonic integrated chip according to claim 7, wherein the second alignment element include a plurality of substantially square cross section columns arranged in a predetermined shape through which a laser beam may pass in use.

9. The photonic integrated chip according to claim 8, wherein there are four columns arranged at the four corners of a substantially square predetermined shape, wherein the columns are separated by gaps there between and wherein the inward facing walls include an third irregular profile.

10. The photonic integrated chip according to any of claims 6 to 9, wherein the or each irregular profile includes a Vernier scale to enable positioning of the laser diode in the predetermined position.

11. The photonic integrated chip according to any preceding claims, wherein the asymmetrical alignment assembly includes one or more stoppers which have a predetermined vertical height for positioning the laser diode relative to the PIC.

12. The photonic integrated chip according to any preceding claims, wherein the coupler is a suspended coupler.

13. The photonic integrated chip according to claim 12 wherein the suspended coupler includes a suspended oxide waveguide and a silicon nano-taper.

14. The photonic integrated chip according to claim 12 or claim 13 comprising a large input facet for the suspended coupler in order to enhance the alignment tolerance when coupling to the laser diode.

15. The photonic integrated chip according to any one of claims 12 to 14, wherein the suspended coupler is isolated from the chip by one or more air-isolation trenches formed by removing the adjacent oxide layer and underlying substrate silicon.

16. The photonic integrated chip according to claim 13, wherein one or more oxide arms 910 are formed to provide a mechanical support for the suspended coupler.

17. The photonic integrated chip according to any one of claims 12 to 16, wherein the silicon nano-taper is designed to couple the light inside oxide waveguide to silicon photonic circuit.

18. The photonic integrated chip according to any one of claims 12 to 17, wherein the coupler includes a tilted face for receiving a laser beam in use.

19. The photonic chip according to claim 18, wherein the tilted face is angled in a vertical direction and a lateral direction.

20. The photonic integrated chip according to any of the preceding claims, including a laser diode in the predetermined position.

21. A method of fabricating a photonic integrated chip, PIC, adapted to receive a laser diode in a predetermined positon, the method comprising:

forming a from a first material a substrate, the substrate comprising an asymmetric alignment arrangement defining the predetermined position;

forming from at least one second material a chip for a function and having an a coupler for receiving a laser beam in use.

22. The method according to claim 21, further comprising:

forming a plurality of alignment keys configured to align the attachment of the laser diode in the predetermined position.

23. The method of any of claims 21 to 22, further comprises:

forming at least one pair of alignment keys to be asymmetric relative to one another.

24. The method of claim 23, further comprising:

forming the pair of alignment keys as elongate elements that run along a direction substantially parallel to the laser beam in use.

25. The method of claim 24, further comprising:

forming the pair of alignment keys to include a gap between them defining a channel.

26. The method of claim 25, further comprising:

forming the gap to include a central region having a uniform profile and two sections at either end, each having a respective first irregular profile and second irregular profile; and

forming the first irregular profile of one of the pair to be juxtaposed to the second irregular profile of the other of the pair.

27. The method according to any one of claims 21 to 26, further comprising forming a second alignment element.

28. The method according to claim 27, further comprising forming the second alignment element to include a plurality of substantially square cross section columns arranged in a predetermined shape through which a laser beam may pass in use.

29. The method according to claim 28, further comprising forming four columns arranged at the four corners of a substantially square predetermined shape, wherein the columns are separated by gaps there between and wherein the inward facing walls include an third irregular profile.

30. The method of any of claims 26 to 29, further comprising: forming the irregular profile to include a Vernier scale which is used to position the laser diode in the predetermined position

31. The method of any of claims 21 to 30, further comprising:

forming one or more stoppers as part of the asymmetrical alignment assembly which stoppers are formed at a predetermined vertical height for positioning the laser diode relative to the PIC.

32. The method of any of claims 21 to 31, further comprising:

forming the coupler as a suspended coupler comprising the steps of:

forming a suspended oxide waveguide; and

forming a silicon nano-taper.

33. The method of claim 32, further comprising:

isolating the coupler by air-isolation trenches formed by removing a adjacent oxide layer and an underlying substrate silicon.

34. The method of claim 33, further comprising: forming one or more pairs of oxide arms to provide the mechanical support for the suspended waveguide.

35. The method of any one of claims 32 to 34, further comprising:

forming the coupler to include a tilted face for receiving a laser beam in use.

36. The method of claim 35 further comprising:

forming the tilted face angled in a vertical direction and a lateral direction.

37. The method according to any of claims 21 to 36, further comprising positioning a laser diode on the alignment arrangement to position the laser diode in the predetermined position.

38. The method of claim 37, further comprising a flip chip process.

39. A process design kit for forming a photonic integrated chip which when processed in a chip fabrication system causes the chip fabrication system to from the photonics integrated chip of any of claims 1 to 20.

40. A computer readable storage medium having stored thereon a computer readable description of a chip that, when processed in chip fabrication system, causes chip fabrication system to manufacture a photonic integrated chip as claimed in any of claims 1 to 20.