

SPECIFICATION

Amplifier arrangement

5 The invention relates to an amplifier arrangement constructed as an integrated circuit, said arrangement comprising first and second transistors arranged as a differential pair to whose base electrodes an input of the arrangement is coupled, whose
10 emitter electrodes are coupled to each other, and whose collector electrodes are coupled to an output of the arrangement and *via* a load circuit to a supply terminal, the load circuit, in order to increase the gain at higher frequencies, comprising third and
15 fourth transistors which are both of the same conductivity type as the first and second transistors, the main current paths of said third and fourth transistors being connected in series with the main current paths of the first and second transistors respectively
20 in that the emitter electrodes of the third and fourth transistors are connected to the collector electrodes of the first and second transistors respectively and the collector electrodes of the third and fourth transistors are connected to said supply terminal *via* first
25 and second impedances respectively, third and fourth impedances being included in the base circuits of the third and fourth transistors respectively.

Such an amplifier arrangement is known from an article by J. Choma entitled "Actively peaked broad-
30 banded monolithic amplifier" in IEE Proceedings, Vol. 127, no. 2, April 1980, pages 61-66 in particular Figure 7. In such an amplifier arrangement the inductive nature of the third and fourth transistors, whose base circuits include the third and fourth im-
35 pedances respectively, is used to increase the gain at specific frequencies in order to compensate for the roll-off which would otherwise occur at higher frequencies owing to transistor characteristics and/or stray capacitances or even in order to peak the gain
40 factor of the arrangement at specific frequencies. In the known arrangement the base electrodes of said third and fourth transistors are connected to a point of constant potential *via* said third and fourth im-
pedances.

45 For various high-frequency applications of such amplifier arrangements, for example in television receiver tuners, the amplifier should exhibit no low-frequency gain. As a result of direct-voltage and low-frequency gain any input direct voltages –
50 caused by unequal settings of the first and the second transistor or by circuits preceding the first and the second transistor – would appear amplified on the output, so that d.c. coupling to a following circuit having a differential input would not be readily possible. Of course a capacitive coupling could be pro-
55 vided to the next circuit, but this would have the drawbacks that the integrated circuit would then have to be provided with additional terminals for the connection of the two capacitors required for this, and that these external components which would
60 then be necessary would result in high-frequency radiation, with a consequent increased risk of instability. If the d.c. gain were to be eliminated by means of low-frequency negative feedback *via* an at least
65 partly external RC-network this would have similar

drawbacks.

Due to said drawbacks it is difficult to combine sensitive high-frequency amplifiers on a single semiconductor substrate with other circuits such as frequency dividers, for example for television tuners.

70 It is an object of the invention to provide an amplifier arrangement of the type set forth in the opening paragraph in which the direct voltage gain can be substantially eliminated without the necessity of providing external components, which arrangement
75 employs a minimum of components and need not dissipate an untoward amount of power.

An arrangement according to the invention is characterized in that the base electrode of the third
80 transistor is connected to the collector electrode of the fourth transistor *via* said third impedance and the base electrode of the fourth transistor is connected to the collector electrode of the third transistor *via* said fourth impedance.

85 In such an arrangement the direct voltage gain can be substantially eliminated by arranging that equal and opposite variations of the direct currents in the collector circuits of the first and second transistors will each compensate, *via* the cross-coupled third and
90 third transistors, for the corresponding voltage variation which would otherwise occur on the collector of the other one of said first and second transistors. The arrangement can still have high-frequency gain because the inductive nature of the third and the
95 fourth transistor will result in the impedance of the load circuit constituted by the third and the fourth transistor increasing with frequency and hence in high-frequency signal current flowing in any load
100 connected between the collectors of the first and second transistors. It will be noted that such an arrangement demands no additional components compared with the aforesaid known arrangement; in fact the number of components can even be reduced because it is not necessary to provide a separate d.c.
105 bias source for the base electrodes of the third and fourth transistors, such a source being required in the known arrangement.

An embodiment of the invention will now be described in detail, by way of example, with reference to the accompanying diagrammatic drawing the single Figure of which is a circuit diagram of the
110 embodiment.

In the Figure an amplifier arrangement constructed as an integrated circuit comprises a first (T_1)
115 and a second (T_2) transistor, which are connected as a differential amplifier in that the emitter electrodes thereof are connected to a quiescent current source 6, which carries a current $2I$, the base electrodes thereof are connected to a differential input 1, 2, and the collector electrodes thereof are connected to an
120 output 3, 4 between which a load 11, having a resistance R_L , is included. Load 11 may be constituted by the input impedance of a following circuit. The collector electrodes of transistors T_1 and T_2 are con-
125 nected to a supply terminal 5 *via* the emitter-collector paths of transistors T_3 and T_4 respectively and impedances 7 and 8 respectively, these impedances each having a resistance R_e in the present example. The base electrode of transistor T_3 is con-
130 nected to the collector of transistor T_4 *via* an impe-

2
 5 dance 10, having a resistance R_b in the present example, and the base electrode of transistor T_1 is connected to the collector of transistor T_2 via an impedance 9, also having a resistance R_b in the present example.

For direct currents and signal currents of comparatively low frequency the emitter input impedances of transistors T_1 and T_2 are low relative to the load 11. The collector direct currents and low-frequency alternating currents of transistors T_1 and T_2 thus mainly flow through the emitter-collector paths of transistors T_1 and T_2 .

If the currents in the collector circuits of transistors T_1 and T_2 are $I+i$ and $I-i$ respectively, in which i is a component arising from an input direct-voltage difference $2V_i$ or from inequality between the transistors T_1 and T_2 , the voltage V_u on output terminal 3 caused by the d.c. component i is given by:

$$V_u = i r_o + R_b \frac{i}{\beta} + R_c \frac{i}{\beta} - i R_c + \frac{i}{\beta} R_c$$

where β is the current gain factor of the transistors T_1 and T_2 , and r_o is the differential d.c. resistance of the base-emitter junctions of transistors T_1 and T_2 . An equal but opposite voltage is produced on output terminal 4. The voltage V_u at terminal 3 is the sum of the voltage $i r_o$ across the base-emitter junction of transistor T_1 , the voltage $i(R_b + R_c)/\beta$, produced across the impedances 10 and 8 by the base current of transistor T_1 , and the (oppositely directed) voltage

$i R_c (1 - \frac{1}{\beta})$ produced across impedance 8 by the collector current of transistor T_2 . This voltage arising from the differential d.c. component i can be made zero by selecting the various parameters in such a way that

$$r_o + \frac{R_b}{\beta} - (1 - \frac{1}{\beta}) R_c = 0.$$

If $r_o = \frac{25 \text{ mV}}{I}$, the requirement for eliminating the

difference in output direct voltage between terminals 3 and 4 will be:

$$I (1 - \frac{1}{\beta}) R_c - \frac{R_b}{\beta} = 25 \text{ mV}.$$

This requirement can be met by a suitable choice of three parameters I , R_c and R_b , any two of which may be selected freely. This leaves sufficient degrees of freedom to enable the high-frequency behaviour of the circuit to be optimized without adversely affecting the elimination of any direct-voltage difference.

For signal currents of higher frequencies the emitter input impedances of the transistors T_1 and T_2 , which when arranged as shown have an inductive nature, increases and an amplified signal voltage is produced across the load 11.

CLAIMS

1. An amplifier arrangement, constructed as an integrated circuit, said arrangement comprising first and second transistors arranged as a differential pair to whose base electrodes an input of the arrangement is coupled, whose emitter electrodes are coupled to each other, and whose collector electrodes are coupled to an output of the arrangement and via a load circuit to a supply terminal, the load circuit, in order to increase the gain at higher frequencies, comprising third and fourth transistors which are both of the same conductivity type as the first and second transistors, the main current paths of said third and fourth transistors being connected in series with the main current paths of the first and second transistors respectively in that the emitter electrodes of the third and fourth transistors are connected to the collector electrodes of the first and second transistors respectively and the collector electrodes of the third and fourth transistors are connected to said supply terminal via first and second impedances respectively, third and fourth impedances being included in the base circuits of the third and fourth transistors respectively, characterized in that the base electrode of the third transistor is connected to the collector electrode of the fourth transistor via said third impedance and the base electrode of the fourth transistor is connected to the collector electrode of the third transistor via said fourth impedance.

2. An amplifier arrangement constructed as an integrated circuit, substantially as described herein with reference to the drawing.

The text of the specification has been reproduced by photocopying. The original typescript may be inspected on the premises of the Patent Office



2
dance 10, having a resistance R_b in the present example, and the base electrode of transistor T_4 is connected to the collector of transistor T_2 via an impedance 9, also having a resistance R_b in the present example.

For direct currents and signal currents of comparatively low frequency the emitter input impedances of transistors T_3 and T_4 are low relative to the load 11.

The collector direct currents and low-frequency alternating currents of transistors T_1 and T_2 thus mainly flow through the emitter-collector paths of transistors T_3 and T_4 .

If the currents in the collector circuits of transistors T_1 and T_2 are $I+i$ and $I-i$ respectively, in which i is a component arising from an input direct-voltage difference $2V_i$ or from inequality between the transistors T_1 and T_2 , the voltage V_o on output terminal 3 caused by the d.c. component i is given by:

$$V_o = i r_o + R_b \frac{i}{\beta} + R_c \frac{i}{\beta} - i R_c + \frac{i}{\beta} R_c$$

where β is the current gain factor of the transistors T_3 and T_4 , and r_o is the differential d.c. resistance of the base-emitter junctions of transistors T_3 and T_4 . An equal but opposite voltage is produced on output terminal 4. The voltage V_o at terminal 3 is the sum of the voltage $i r_o$ across the base-emitter junction of transistor T_3 , the voltage $i(R_b + R_c)/\beta$, produced across the impedances 10 and 8 by the base current of transistor T_3 , and the (oppositely directed) voltage

$i R_c (1 - \frac{1}{\beta})$ produced across impedance 8 by the collector current of transistor T_4 . This voltage arising from the differential d.c. component i can be made zero by selecting the various parameters in such a way that

$$r_o + \frac{R_b}{\beta} - (1 - \frac{1}{\beta}) R_c = 0$$

If $r_o = \frac{25 \text{ mV}}{I}$, the requirement for eliminating the

difference in output direct voltage between terminals 3 and 4 will be:

$$I (1 - \frac{2}{\beta}) R_c - \frac{R_b}{\beta} = 25 \text{ mV.}$$

This requirement can be met by a suitable choice of three parameters I , R_c and R_b , any two of which may be selected freely. This leaves sufficient degrees of freedom to enable the high-frequency behaviour of the circuit to be optimized without adversely affecting the elimination of any direct-voltage difference.

For signal currents of higher frequencies the emitter input impedances of the transistors T_3 and T_4 , which when arranged as shown have an inductive nature, increases and an amplified signal voltage is produced across the load 11.

CLAIMS

1. An amplifier arrangement, constructed as an integrated circuit, said arrangement comprising first and second transistors arranged as a differential pair to whose base electrodes an input of the arrangement is coupled, whose emitter electrodes are coupled to each other, and whose collector electrodes are coupled to an output of the arrangement and via a load circuit to a supply terminal, the load circuit, in order to increase the gain at higher frequencies, comprising third and fourth transistors which are both of the same conductivity type as the first and second transistors, the main current paths of said third and fourth transistors being connected in series with the main current paths of the first and second transistors respectively in that the emitter electrodes of the third and fourth transistors are connected to the collector electrodes of the first and second transistors respectively and the collector electrodes of the third and fourth transistors are connected to said supply terminal via first and second impedances respectively, third and fourth impedances being included in the base circuits of the third and fourth transistors respectively, characterized in that the base electrode of the third transistor is connected to the collector electrode of the fourth transistor via said third impedance and the base electrode of the fourth transistor is connected to the collector electrode of the third transistor via said fourth impedance.

2. An amplifier arrangement constructed as an integrated circuit, substantially as described herein with reference to the drawing.

The text of the specification has been reproduced by photocopying. The original typescript may be inspected on the premises of the Patent Office