

LEADED MCM PACKAGE AND METHOD THEREFOR

This invention relates generally to the field of semiconductor device manufacture and more particularly to the packaging of semiconductor devices with integrated circuit chips to be used in an electronic assembly, such as a printed circuit board.

In the electronics industry, the quest for smaller electronic devices which perform better at a lower cost is ongoing. This is especially true of the portable electronics and wireless communications sector which has undergone recent rapid growth. In particular, there is often a need for a single semiconductor package which can perform a variety of diverse functions with high performance.

Generally speaking, two different technologies which are able to provide complete electronic systems in a single package may be identified. The first technology is known as system-on-a-chip (SoC). This technology involves integrating several integrated circuits having different functions (such as memory, logic, analog etc) into a single composite chip at the die level. The resultant single chip is generally smaller in size than the combined size of individual component integrated circuits. Further, the system performance is generally superior due to the shorter electrical paths and lower electrical parasitics between the component integrated circuits.

The second technology is known as system-in-a-package (SiP) which involves packaging several discrete integrated circuit chips in a single package. In common with SoC, the main objective of SiP is to minimize the required form factor of the IC components on the systems board while increasing the systems functionality and performance.

In recent times, SiP has become increasingly popular compared to the SoC solution because it benefits from a number of additional advantages. In particular, SiP packages are easier to produce than SoC chips and usually they are more cost effective and have a shorter time-to-market.

The SiP technology can be further broken down into two sub-types of MCM (multi-chip module) or MCP (multi-chip package). The distinction between MCM

and MCP lies mainly in the type of substrate used and the number of IC components in the total package. A MCM generally has larger substrates with higher densities of various materials (ceramic, thin-film, laminate) and uses different types of die attachment methods (flip chip, TAB, wire bond) within the same package. In

5 contrast, a MCP uses a cheaper substrate material (usually laminates) and has a fewer number of component dies (about 2-3). Interconnects are usually made by wire bonding but flip chip interconnect is also possible. Furthermore, the pin count of MCPs is usually lower than the pin count of MCMs.

The substrates used in MCPs and MCMs are generally ball grid arrays
10 (BGAs) or land grid rays (LGAs). It would, however, be desirable to have leaded MCM/MCPs so that manufactures who want to adopt SiP for their semiconductor devices can comply with leaded packaging formats. A leaded package offers much better solder joint fatigue reliability compared to a leadless package such as LGA or BGA. In particular, the leads of the leaded package provide for more solder
15 attachment compliance to accommodate expansion mis-match between the package and the board during thermal cycling. For leadless packages such as LGA, the attachment compliance is much lower, resulting in a poorer soldered joint fatigue reliability.

The present invention relates to a novel semiconductor package using SiP
20 technology with leads. Further, the present invention relates to a method of packaging a leaded multi-chip package.

Accordingly, the present invention provides a method of packaging a semiconductor device, said method comprising:

providing a substrate having a plurality of exposed conductive traces thereon;
25 attaching an integrated circuit chip to said substrate;
electrically connecting a bond pad on said integrated circuit chip with one of said exposed conductive traces;
attaching a metallic leadframe to said substrate;
electrically connecting said metallic leadframe to one of said conductive
30 traces so as to provide an electrical pathway between said integrated chip and said metallic leadframe;

encapsulating said integrated circuit chip, said substrate and said electrical connections in a moulding compound.

The invention enables multiple integrated circuit chips having different functions and passive components (such as capacitors, resistors etc.) to be packaged
5 in leaded packages, using a combination of substrate and leadframe. A leadframe die paddle is not required in a device manufactured according to the present invention. The invention therefore represents a feasible option for manufacturers who would like to adopt system-in-package technology using leaded packages. The invention provides a compact and easy to manufacture package available at low cost. The
10 invention provides a leaded multi-chip package that is compatible with the existing surface mount assembly application. Furthermore, the present invention also enables manufacturers to advance to a system-in-package platform for their devices without having to make major changes to their existing test and surface mount assembly infrastructure. This is because the method of the present invention uses a
15 combination of different techniques readily achievable with conventional and widespread technology.

Preferably, the method also comprises attaching at least one passive component on the substrate. Preferably, a plurality of exposed conductive traces are formed by printing a thin layer of conductive material onto said substrate, covering in
20 soldermask material and removing selected areas of said soldermask material to expose portions of the conductive material.

Preferably, bond wires are attached between the bond pads on the integrated chips and bond fingers on the conductive traces.

The metallic leadframe is preferably attached to the substrate by especially
25 provided parts which will not be used as external connections. The metallic leadframe is preferably attached to the substrate using an adhesive tape. Further, the metallic leadframe may be connected to bond fingers on the conductive traces using a bonding wire. In one embodiment, the integrated circuit and leadframe are electrically connected to the same conductive trace. Alternatively, they can be
30 connected to two different conductive traces which are themselves electrically

connected. As a further alternative, the integrated circuit and leadframe may be directly connected.

Preferably, the parts of the metallic leadframe which are visible after moulding are bent or otherwise formed into various shapes, such as a gull-wing
5 shape a straight leg shape or a J-shape.

The present invention also provides a semiconductor package comprising:
a substrate:

- an integrated circuit chip attached to said substrate,
- a bond pad on said integrated circuit chip;
- 10 a plurality of conductive traces on said substrate;
- a first connector connecting said bond pad to a conductive trace;
- a metallic leadframe attached to said substrate;
- a second connector which electrically connects said metallic leadframe to one
of said conductive traces to create an electrical pathway between said integrated
15 circuit chip and said leadframe;

moulding compound which encapsulates said substrate, said integrated circuit chip and said first and second connectors.

The substrate is preferably formed of a plurality of layers which are laminated together. Further, the substrate preferably comprises printed conductive traces and a
20 layer of soldermask on top of these traces. Portions of the soldermask are removed so as to reveal portions of the printed conductive traces underneath.

A layer of adhesive tape is preferably present to adhere the substrate to the metallic leadframe.

The present invention also encompasses a printed circuit board or electronic
25 device which comprises a semiconductor package as claimed or a semiconductor package manufactured according to the claimed method.

The present invention will now be described by way of non-limitative example only, with reference to the accompanying schematic drawings, in which:-

Figures 1-5 show in perspective view successive steps in a method of
30 packaging a semiconductor device according to the present invention;

Figure 6 shows three final semiconductor packages in side view constructed in accordance with three respective embodiments of the present invention.

Detailed embodiments of the invention will now be described.

5 Figures 1-5 schematically illustrate the method steps of the present invention and these will now be described.

Figure 1 shows a laminated substrate (1) which is a printed circuit substrate in this embodiment. Conductive traces are printed on the top side of the substrate (1). The conductive traces are in turn covered with a layer of soldermask material which
10 has had some designated areas removed so as to reveal parts of the metallic conductive traces and leave exposed rectangular portions of the traces (2,3). It is to be noted that the exact shape of these traces is not material to the present invention. The exposed portions shown in Figure 1 may be labelled as outer traces (2) and inner traces (3). The underlying pattern of conductive traces is not shown in the Figures
15 but it is to be understood that any useful pattern may be applied, for example, in the present embodiment, the pattern is such that each of the inner traces (3) is electrically connected to a respective one of the outer traces (2).

As is shown in Figure 2, a plurality of integrated circuit chips (4,5) and a passive component (6) are attached to the substrate (1) using an adhesive such as
20 epoxy die attach paste or adhesive film. Usually, the passive components are soldered to designated traces on the substrate prior to leadframe mounting. However, the passive components may be attached after the leadframe is mounted and either before or after the integrated circuits are mounted. These integrated circuit chips (4,5) and passive components (6) may perform substantially any function, such as
25 memory, logic, analog electronics etc. The integrated circuit chips have bond pads (15) located on their top surfaces. These pads (15) are used for receiving/transmitting electrical signals from the integrated chip to the outside world.

The passive components (6) are applied to the substrate by using solder paste to tack the passive components to the designated conductive traces. The solder paste
30 is then subject to reflow which causes the solder paste to form a solder joint with the passive component.

In the next step shown in Figure 3, a metallic leadframe (7) is attached to the top surface of the substrate (1) using the T-shaped attachment portions (8) by means of non-conductive adhesive film, such as polyimide tape. Here, the T-shaped portions are especially provided for the purpose of attaching the leadframe (7) to the substrate (1) but it should be understood that an extended lead of the leadframe (7) may be provided for this purpose in which case it would have the dual function of connecting the leadframe (7) to the substrate (1) during assembly as well as routing electrical signals during use of the final package. In this embodiment, the leadframe attachment portions are attached to a portion of the substrate (1) having no exposed conductive traces (2,3) or any chips (4,5) or passive components (6). However, any suitable adhesive mixture/device may be used. The purpose of the leadframe (7) is to provide external electrical contacts for the whole package so that electrical signals may be routed to and from the integrated circuit chips (4,5) and passive component (6) on the first (top) side of the substrate (1).

It should be noted that the integrated circuit chips (4,5) and passive components (6) may be mounted to the substrate (1) after the leadframe (7) has been mounted. The Figures show the other order of assembly simply as an example.

Figure 4 shows the device after the next step has been performed, namely, connecting the chips/passive components to the leadframe (7) using bonding wires. Bond fingers are used on the conductive traces (2,3) to connect the (preferably gold) bonding wire to the conductive trace. In this way, each bond pad (15) on the integrated circuit may be connected to a leadframe finger via at least one conductive trace (2,3) on the substrate (1). The bonds between the bond wires and conductive traces are made by soldering in much the same way as the passive components (6) are connected to the conductive traces. Figure 4 shows three examples of connections between the leadframe and the integrated circuits. The right side of first integrated circuit chip (5) has its bond pads (15) connected to the outer traces (2) by means of bond wires (9). Similarly the leadframe fingers are connected to the same outer traces (2) by means of similar bond wires (10). The same outer trace (2) thus has two wires (9,10) attached to two respective bond fingers located on it. The left side of the integrated chip (5) has its bond pads (15) directly connected to leadframe

fingers by means of bond wires (16). On the other hand, the second integrated circuit chip (4) is connected to the inner traces (3) by means of bonding wires (9) and the inner traces (3) are connected to respective ones of the outer traces (5) by means of the pattern of conductive traces lying under the soldermask material. In turn, the
5 outer traces (2) are connected to the leadframe fingers using wires (10). Thus, each exposed trace (2,3) only has a single bonding wire connection and thus only requires a single bond finger.

After the connections have been made, moulding compound (11) is used to encapsulate all the components on the top side of the substrate (1) and part of the
10 leadframe fingers. This protects all the components both physically and electrically.

The outer supporting part of the leadframe (7) is then removed so that all the leadframe fingers (which were all electrically connected due to the outer leadframe portion) become electrically isolated and independent. These fingers become the external leads of the package and may be bent into a useful shape as shown in Figure
15 6. Figure 6 shows three different embodiments where the external leads are bent so as to be formed into the shape of a gull-wing (12), a straight lead (13) or a J-shape (14) respectively.

The above methods may be carried out using components manufactured of
20 materials standard in the art. Examples of materials which can be used for the various components are:

Component	Material
Substrate	Bismaleimide Triazine resin or FR4
25 Conductive Traces	Copper with Nickel/Gold finish
Soldermask Material	Photo-imageable dielectric resist (for example Taiyo PSR 4000)
Bonding Wires	Gold
Moulding Compound	Epoxy resin based with silica fillers
Adhesive Tape	Epoxy based



CLAIMS

1. A method of packaging a semiconductor device, said method comprising:
 - 5 providing a substrate having a plurality of exposed conductive traces thereon;
attaching an integrated circuit chip to said substrate;
electrically connecting a bond pad on said integrated circuit chip with one of
said exposed conductive traces;
attaching a metallic leadframe to said substrate;
 - 10 electrically connecting said metallic leadframe to one of said conductive
traces so as to provide an electrical pathway between said integrated chip and said
metallic leadframe;
encapsulating said integrated circuit chip, said substrate and said electrical
connections in a moulding compound.
- 15 2. A method according to claim 1, wherein at least one passive
component is attached to said substrate.
- 20 3. A method according to claim 1 or 2, wherein said plurality of exposed
conductive traces are formed by printing a thin layer of conductive material onto said
substrate, covering in soldermask material and removing selected areas of said
soldermask material to expose portions of the conductive material.
- 25 4. A method according to any one of the preceding claims, wherein at
least one of said steps of electrically connecting comprises connecting with a bond
wire.
- 30 5. A method according to claim 4, wherein said step of electrically
connecting further comprises providing a bond finger on said conductive trace to
which said bond wire is to be attached.



6. A method according to any one of the preceding claims, wherein said metallic leadframe is attached to said substrate by parts of the leadframe which are not destined to carry any electrical current.

5 7. A method according to any one of claims 1 to 5, wherein said leadframe is attached to said substrate by fingers which are destined to carry current to/from said integrated circuit chips.

8. A method according to any one of the preceding claims, wherein said
10 metallic leadframe is attached to said substrate using an adhesive tape.

9. A method according to any one of the preceding claims, wherein said integrated circuit chip is connected to a first conductive trace and said metallic leadframe is connected to a second conductive trace, an electrical pathway being
15 made between said integrated circuit chip and said leadframe by an electrical connection on said substrate located between said first and second conductive traces.

10. A method according to any one of claims 1 to 8, wherein said integrated circuit chip and said metallic leadframe are both connected to the same
20 conductive trace on the substrate.

11. A method according to any one of the preceding claims, wherein a plurality of integrated circuit chips are provided on said substrate.

25 12. A method according to any one of the preceding claims, wherein said step of encapsulating comprises encapsulating the device with moulding compound leaving revealed those parts of the metallic leadframe which are destined to become external connections.



13. A method according to any one of the preceding claims, further comprising removing a portion of the metallic leadframe to create independent external connections.

5 14. A method according to claim 13, further comprising bending or otherwise forming the external connections into a predetermined shape.

15. A semiconductor package comprising:
a substrate:
10 an integrated circuit chip attached to said substrate,
a bond pad on said integrated circuit chip;
a plurality of conductive traces on said substrate;
a first connector connecting said bond pad to a conductive trace;
a metallic leadframe attached to said substrate;
15 a second connector which electrically connects said metallic leadframe to one of said conductive traces to create an electrical pathway between said integrated circuit chip and said leadframe;
moulding compound which encapsulates said substrate, said integrated circuit chip and said first and second connectors.

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16. A semiconductor package according to claim 15, wherein said substrate is formed of a plurality of layers laminated together.

17. A semiconductor package according to claim 15 or 16, wherein said
25 conductive traces are printed on said substrate.

18 A semiconductor package according to any one of claims 15 to 17, further comprising a layer of adhesive tape between said substrate and said metallic leadframe.

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19. A semiconductor package according to any one of claims 15 to 18,
further comprising at least one passive electrical component on said substrate.

20. A semiconductor package according to any one of claims 15 to 19,
5 wherein said first and second connectors are bond wires.

21. A semiconductor package according to claim 20, further comprising
bond fingers on said conductive traces for attaching to said bond wires.

10 22. A semiconductor package according to any one of claims 15 to 21,
wherein said metallic leadframe is connected to said substrate via portions of said
metallic leadframe which are not electrically connected to said conductive traces.

23. A semiconductor package according to any one of claims 15 to 22,
15 wherein said metallic leadframe is attached to said substrate via portions which are
electrically connected to said conductive traces.

24. A semiconductor device according to any one of claims 15 to 23,
wherein said bond pad and said metallic leadframe are each connected to the same
20 conductive trace.

25. A semiconductor device according to any one of claims 15 to 23,
wherein said bond pad and said metallic leadframe are connected to different
conductive traces, the electrical pathway therebetween being completed by an
25 electrical connection between the two conductive traces.

26. A semiconductor package according to any one of claims 17 to 25,
wherein said metallic leadframe has trimmed external portions which are gull-wing
shaped, straight or J-shaped.

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27. A printed circuit board comprising a semiconductor package according to any one of claims 15 to 26 or a semiconductor device packaged according to the method of any one of claims 1 to 14.

5 28. An electronic device comprising a semiconductor package according to any one of claims 15 to 26 or a semiconductor device packaged according to the method of any one of claims 1 to 14.

29. A method of packaging a semiconductor substantially as hereinbefore
10 described with reference to Figures 1 to 6 of the accompanying drawings.

30. A semiconductor package constructed and arranged substantially as hereinbefore described with reference to Figures 1 to 6 of the accompanying drawings.