

CLOCK CIRCUIT AND MEMORY

ABSTRACT

Provided are a clock circuit and a memory. The clock circuit comprises: a data gating clock module for receiving a data gating clock signal and transmitting the data gating clock signal, wherein the data gating clock signal is used for controlling the receiving and/or sending of a data signal; a system clock module for receiving a system clock signal and transmitting the system clock signal, wherein the system clock signal is used for controlling the receiving of a command signal, and the system clock module comprises at least two first signal transmission paths, and is configured to transmit the system clock signal by using a different first signal transmission path according to a different receiving rate and/or sending rate of the data signal.

[Fig. 6]