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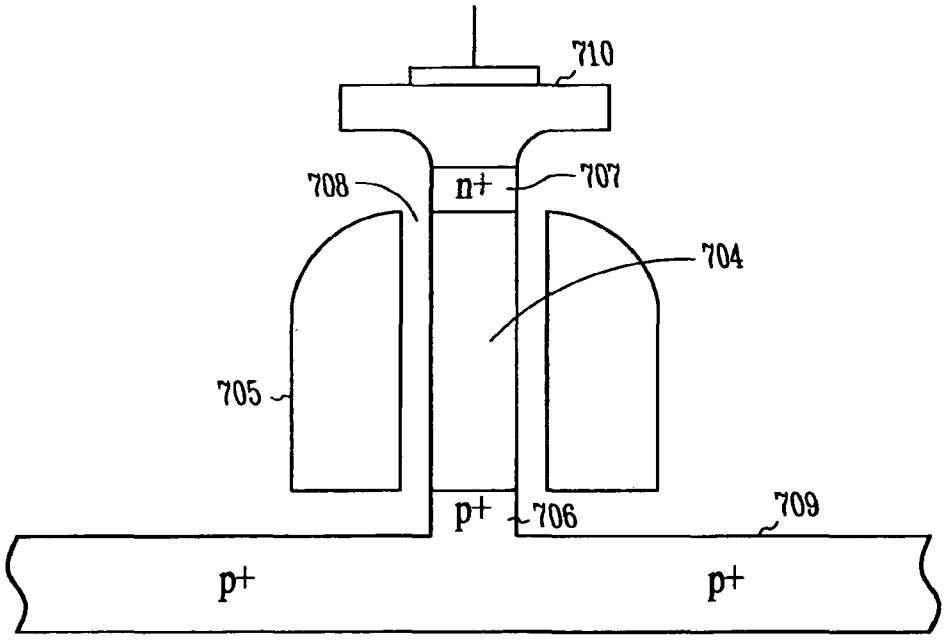
(54) Title: NANOFIN TUNNELING TRANSISTORS



(57) Abstract: Disclosed herein are vertical tunneling transistors with gates that surround transistor bodies that have a width dimension less than a photolithographic dimension. These thin tunneling transistors with surrounding gates are used to obtain low sub-threshold leakage. Various embodiments provide sublithographic bodies by growing a crystalline nanofin from an amorphous structure formed on a substrate, by etching a crystalline substrate to define a crystalline nanofin from the crystalline substrate, or by growing a crystalline nanowire from an amorphous structure formed on the substrate. Other aspects and embodiments are provided herein.

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