CLAIMS

1. A semiconductor wafer, comprising:

a surface having at least one recess including an inner wall surface and a bottom surface, the inner wall surface and the bottom surface being exposed, wherein:

the at least one recess includes a first recess and a second recess;

the first recess extends along a first direction of the surface;

the second recess extends along a second direction intersecting with the first direction on the surface; and

each of the first and second recesses is surrounded by the corresponding inner wall surface.

2. The semiconductor wafer according to claim 1, wherein

the at least one recess has a depth from the surface of 20 μm or more and an aspect ratio of 50 or more.

3. The semiconductor wafer according to claim 1 or claim 2, wherein

a surface area of the surface is 50 times or more a surface area of a surface opposite to the surface.

4. The semiconductor wafer according to any one of claims 1 to 3, wherein

the at least one recess is provided via a partition.

5. The semiconductor wafer according to any one of claims 1 to 4, wherein

the surface further has a porous region.

6. The semiconductor wafer according to any one of claims 1 to 5, wherein the surface further has a protrusion provided in the at least one recess.

7. The semiconductor wafer according to any one of claims 1 to 6, further comprising

a film provided on the surface.

8. The semiconductor wafer according to claim 7, wherein

the film contains silicon carbide or silicon carbonitride.

9. The semiconductor wafer according to any one of claims 1 to 8, wherein the semiconductor wafer is a silicon wafer, a silicon carbide wafer, a glass wafer, a quartz wafer, a sapphire wafer, or a compound semiconductor wafer.

10. The semiconductor wafer according to claim 9, wherein

the semiconductor wafer is the silicon wafer.

11. The semiconductor wafer according to any one of claims 1 to 10, wherein the surface is a (110) plane.

12. A method of manufacturing a semiconductor apparatus, comprising:

placing a first semiconductor wafer into a chamber, the first semiconductor wafer including a first surface and a film provided on the first surface, the film having a first recess;

placing a second semiconductor wafer into the chamber, the second semiconductor including a second surface having a second recess, the second recess

including an inner wall surface and a bottom surface, the inner wall surface and a bottom surface being exposed, the second recess including a third recess and a fourth recess, the third recess extends along a first direction of the second surface, the fourth recess extending along a second direction intersecting with the first direction on the second surface, and each of the first and second recesses being surrounded by the corresponding inner wall surface; and

simultaneously processing the first and second semiconductor wafers in the chamber.

13. The method according to claim 12, wherein

the film has first layers and second layers, each first layer and each second layer being alternately stacked.

14. The method according to claim 12 or claim 13, wherein

the simultaneous processing includes at least one processing selected from the group consisting of film formation processing, etching process, and modification treatment.

15. The method according to any one of claims 12 to 14, wherein

a plurality of the second semiconductor wafers are placed into the chamber.

16. The method according to any one of claims 12 to 15, wherein

the second recess has a depth from the second surface of 20 μm or more and an aspect ratio of 50 or more.

17. The method according to any one of claims 12 to 16, wherein

a surface area of the second surface is 50 times or more a surface area of a surface opposite to the second surface.

18. The method according to any one of claims 12 to 17, wherein the second recess is provided via a partition.

19. The method according to any one of claims 12 to 18, wherein the second surface further has a porous region.

20. The method according to any one of claims 12 to 19, wherein the second surface further has a protrusion provided in the second recess.

21. The method according to any one of claims 12 to 20, wherein the second semiconductor wafer includes a third film provided on the second surface.

22. The method according to claim 21, wherein the third film contains silicon carbide or silicon carbonitride.

23. The method according to any one of claims 12 to 22, wherein the second semiconductor wafer is a silicon wafer, a silicon carbide wafer, a glass wafer, a quartz wafer, a sapphire wafer, or a compound semiconductor wafer.

24. The method according to claim 23, wherein the second semiconductor wafer is the silicon wafer.

25. The method according to any one of claims 12 to 24, wherein the second surface is a (110) plane.

26. A method of manufacturing a semiconductor wafer, comprising:

forming a catalyst layer onto a surface of a semiconductor substrate, the catalyst layer containing at least one precious metal element selected from the group consisting of gold, silver, platinum, iridium, and palladium;

immersing the semiconductor substrate with the catalyst layer in an etching solution to partly etch the semiconductor substrate and thus form a recess on the surface; and

removing the catalyst layer from the surface.

27. The method according to claim 26, wherein

the semiconductor wafer is a silicon wafer.