

ABSTRACT

SRAM RESISTOR TAB DOPING BY PLUG IMPLANT FROM BURIED CONTACT

A new method of forming a back diffused resistive load element is achieved. A pattern of gate electrodes and interconnection lines is formed overlying a semiconductor substrate. Source and drain regions are formed within the semiconductor substrate. An interpoly oxide layer is deposited overlying the top surfaces of the semiconductor substrate and etched away where it is not covered by a mask to provide an opening to a drain region within the semiconductor substrate and exposing a portion of a gate electrode wherein a spacer comprising interpoly oxide is left on the sidewall of the exposed gate electrode within the opening. In order to remove the interpoly oxide spacer, the interpoly oxide layer is overetched whereby the top portion of the drain region in the semiconductor substrate is etched away along with a portion of the dopant. First ions are implanted into the drain region and the exposed portion of the gate electrode. A third layer undoped polysilicon is deposited over the surface of the interpoly oxide and within the opening and patterned. During subsequent processing, the first ions implanted into the drain region and the exposed portion of the gate electrode diffuse into the third layer of polysilicon and into the substrate increasing the drain junction depth. The third polysilicon layer forms the resistive load element. Seconds ions are implanted into the third polysilicon layer to define a resistor value.

FIGURE 1 IS SUGGESTED FOR PUBLICATION