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SPECIFICATION

Semiconductor device and manufacturing process thereof

TECHNICAL FIELD

This invention relates to a semiconductor device with a shared contact structure and a manufacturing process thereof. The term "shared contact structure" refers to an interconnection structure in which adjacent conductive layers are interconnected via a conductive plug within a single contact hole.

BACKGROUND ART

With the development of semiconductor devices highly integrated and of higher performance such as an LSI, for example, in an MOS type transistor, there have been various attempts in designing a gate electrode and a wiring structure. For example, in an SRAM (Static Random Access Memory), there has been employed a shared contact structure where a gate electrode and a source-drain region are interconnected in a conductive plug within a single contact hole.

Figure 3 shows an example of a semiconductor device with a shared contact structure. In the part A of the figure, a contact hole is opened in an insulating film 3 extending over a gate electrode 22 and an adjacent source-drain region 12, a conductive plug 61 made of, e.g., tungsten is formed in the hole. The gate electrode 22 and the adjacent source-drain region 12 are interconnected via the conductive plug 61.

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In the part B, a conductive plug 62 is formed as with the above conductive plug 61 just over which there is formed a conductive plug 15, over which further a lower wiring 7 in the two-layer wiring structure is formed. The lower wiring 7, the gate electrode 22 and the source-drain region 12 are interconnected via the conductive plugs 62 and 15.

In other words, in the semiconductor device in Figure 3, if a conductive film for the lower wiring 7 is formed directly on the insulating film 3 the upper surface of the conductive plug 61 in the part A is damaged during etching the conductive film. Therefore, on the insulating film 3 there is formed a further insulating film 14, on which the conductive film for the lower wiring 7 is formed. The conductive plug 15 is formed in the insulating film 14.

Thus, in a semiconductor device with a shared contact structure such as in the part A in Figure 3, there are an increased number of manufacturing steps for preventing damages on the upper surface of the conductive plug 61 in forming the lower wiring 7. It has been, therefore, needed to reduce the number of manufacturing steps in a process for manufacturing such a semiconductor device.

An objective of this invention is to prepare a semiconductor device with a shared contact structure such as in the part A in Figure 3, i.e., a shared contact structure without interconnection of wiring over a conductive plug connecting adjacent conductive layers by a process which does not cause damages in the conductive plug, with a reduced number of steps compared with the prior art.

DISCLOSURE OF THE INVENTION

This invention provides a semiconductor device wherein adjacent conductive layers are interconnected via a conductive plug in a single contact hole formed in an interlayer dielectric, a wiring layer is formed just over the interlayer dielectric, and the upper surface of the conductive plug which is not connected to the wiring layer is covered by a conductive coating isolated from the wiring layer.

An embodiment of this invention is a semiconductor device wherein the coating is formed by etching the conductive film for the wiring layer, simultaneously with the wiring layer.

Another embodiment of this invention is a semiconductor device wherein the conductive plug is mainly made of tungsten, and the coating is mainly made of aluminum.

A further embodiment of this invention is a semiconductor device wherein the whole upper surface of the coating is covered by an insulating film.

A further embodiment of this invention is a semiconductor device wherein the conductive plug covered by the coating interconnects a gate electrode in an MOS type transistor with an adjacent source-drain region.

This invention also provides a process for manufacturing a semiconductor device comprising a contact hole forming step for forming an interlayer dielectric on a semiconductor substrate including an area where adjacent conductive layers are formed and then a contact hole is formed such that the upper surfaces of both the conductive layers are exposed in

the interlayer dielectric; a conductive plug forming step for forming a conductive plug in the contact hole; a conductive film forming step for forming a conductive film over the interlayer dielectric; and a wiring layer forming step for forming a wiring layer by etching the conductive film, characterized in that in the conductive film forming step, the conductive film is formed just over the conductive plug and the interlayer dielectric, and in the wiring layer forming step, a coating isolated from the wiring layer is formed, by etching the conductive film, over the conductive plug which is not connected to the wiring layer, simultaneously with forming the wiring layer.

According to the process, the conductive film for the wiring layer is formed just over the conductive plug, but in etching the conductive layer, the coating isolated from the wiring layer is formed over the conductive plug which is not connected to the wiring layer, so that no damages are caused in the upper surface of the conductive plug during the etching.

Therefore, it can eliminate the steps for preventing damages in the conductive plug in the prior art; that is, the steps for forming a further insulating film over the insulating film in which the conductive plug is formed, forming a contact hole on the further insulating film for connection with the wiring layer, and forming a conductive plug in the contact hole.

An embodiment of this invention is a process for manufacturing a semiconductor device wherein the conductive

plug is mainly made of tungsten and the coating is mainly made of aluminum.

Another embodiment of this invention is a process for manufacturing a semiconductor device wherein the whole upper surface of the coating is covered by an insulating film.

This invention also provides a process for manufacturing a semiconductor device comprising an element forming step for forming a gate electrode and a source-drain region of an MOS type transistor on a semiconductor substrate, a first interlayer dielectric forming step for forming a first interlayer dielectric on the substrate after the element forming step, a contact hole forming step for forming a contact hole in the first interlayer dielectric such that the upper surfaces of the gate electrode and the adjacent source-drain region are exposed, a conductive plug forming step for forming a conductive plug in the contact hole, a conductive film forming step for forming a conductive film over the first interlayer dielectric, and a wiring layer forming step for forming a wiring layer by etching the conductive film, characterized in that in the conductive film forming step, the conductive film is formed just over the conductive plug and the first interlayer dielectric; in the wiring layer forming step, a coating isolated from the wiring layer is formed, by etching the conductive film, over the conductive plug which is not connected to the wiring layer, simultaneously with forming the wiring layer; and after the wiring layer forming step, a second interlayer dielectric is formed just over the wiring layer and the coating.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a partial cross section view showing an area around a semiconductor substrate surface for sequentially illustrating the steps of a process for manufacturing a semiconductor device according to an embodiment of this invention;

Figure 2 is a plan view of Figure 1(b); and

Figure 3 is a partial cross section view showing an area around a semiconductor substrate surface for illustrating a prior example of a semiconductor device with a shared contact structure.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of this invention will be described.

Figure 1 is a partial cross section showing an area around a semiconductor substrate surface for sequentially illustrating the steps of a process for manufacturing a semiconductor device according to an embodiment of this invention. Referring to this figure, the process of this embodiment will be described.

First, on a semiconductor substrate 1 is formed elements comprising a gate electrode 22 and a source-drain region 12 in an MOS type transistor.

Specifically, on the surface of the semiconductor substrate 1 are formed a field oxide film and a trench to be conducted a step of separating elements. A gate oxide film 21 and a two-layer structure of gate electrode 22 (22a, 22b)

are formed on predetermined areas in a region where an element is to be formed (an element-forming region). Predetermined areas in the element-forming region are doped to form impurity diffusion layers 11 to 13. An insulating film 23 is then formed, which is in contact with the side faces of the gate electrode 22 and the gate oxide film 21 as well as the upper surface of the impurity diffusion layer 13. The impurity diffusion layers 11 and 12 are further doped to make these layers high-level diffusion layers.

On the semiconductor substrate 1 is then formed an insulating film (a first interlayer dielectric) 3. Then, photolithography-etching step is conducted to insulating film 3 to form contact holes 41, 42 and 5. In an area, of the insulating film 3, in contact with the gate electrode 22 and the adjacent source-drain region 12, the contact holes 41, 42 are formed such that the upper surfaces of the gate electrode 22 and the source-drain region 12 are exposed, while in an area corresponding to the impurity diffusion layer 11, a common contact hole 5 is formed. Figure 1(a) shows a status after the contact holes forming step.

A barrier layer made of Ti or TiN is formed on the sides and the bottoms of the individual contact holes and the upper surface of the insulating film 3. On the barrier layer is deposited a tungsten film by CVD. Then, the tungsten film on the insulating film 3 is removed by plasma etching, and tungsten is left in the contact holes only. Thus, conductive plugs 61, 62, 63 made of tungsten are formed in the contact holes 41, 42, 5, respectively.

The conductive plug 61 connects the gate electrode 22 and the adjacent source-drain region 12 (adjacent conductive layers), but the conductive plug 61 is not connected on the lower wiring 7. On the other hand, the conductive plug 62 connects the gate electrode 22 and the adjacent source-drain region 12 as well as the lower wiring 7 thereon. The conductive plug 63 connects the impurity diffusion layer 11 and the lower wiring 7 thereon.

An aluminum film (a conductive film as a wiring layer) is formed just over the conductive plugs 61 to 63 and the insulating film 3. Photolithography-etching step to the aluminum film is conducted using a mask having an wiring pattern for the lower wiring 7 and a pattern for the coating 8 covering the upper surface of the conductive plug 61. As the aluminum film, an aluminum alloy film containing Si or Si and Cu as alloy components may be appropriately selected. Etching of the aluminum film is conducted using, for example, a mixed gas of BCl_3 and Cl_2 as an etching gas.

Thus, the lower wiring 7 and the coating 8 are formed on the insulating film 3 and the conductive plugs 61 to 63. Figure 1(b) shows the status after the wiring layer forming step. Figure 2 is a plan view of Figure 1(b).

As shown in Figure 2, the lower wiring 7 extends in a plane like a circuit because it is connected to other wirings and conductive layers. On the other hand, the coating 8, which is isolated from the lower wiring 7, covers the upper surface of the conductive plug 61.

Thus, in etching the conductive film for the lower wiring 7, the conductive film on the conductive plug 61 which is not connected to the lower wiring layer 7 is not etched and remains as a coating 8 isolated from the lower wiring 7. Therefore, in the upper surface of the conductive plug 61 which is not connected to the lower wiring 7, no damages are caused by an etching gas in forming the lower wiring 7.

Then, an insulating film (a second interlayer dielectric) 18 is formed on the lower wiring 7 and the coating 8. In the insulating film 18 are formed contact holes for connecting an upper interconnection 9, and conductive plugs 81 are formed in the individual contact holes as described above. Subsequently, the upper interconnection 9 is formed on the insulating film 18 as usual. Thus, a semiconductor device shown in Figure 1(c) is provided.

According to this embodiment, no damages are caused in the upper surface of the conductive plug 61 which is not connected to the lower wiring 7 in the etching step during forming the lower wiring 7, as described above. Therefore, interconnection between the gate electrode 22 and the adjacent source-drain region 12 via the conductive plug 61 is ensured in this semiconductor device.

The planar shape of the coating 8 may be such that the coating covers the whole upper surface of the conductive plug 61. A shape such that the peripheral insulating film 3 is also covered to a predetermined width may be preferable because it can further surely prevent damages on the conductive plug 61. The dimension of the part of the coating 8 extending from

the conductive plug 61 (L1 in Figure 2) corresponds to, for example, 30 to 80 %, preferably 60 % of the dimension of the conductive plug 61 (L in Figure 2).

Comparing the semiconductor device in Figure 1(c) with that in Figure 3 according to the prior art, Figure 3 has an insulating film 14 comprising a conducting plug 15 while Figure 1(c) does not. Furthermore, Figure 1(c) has a coating 8 while Figure 2 does not. Thus, the semiconductor device in Figure 1(c) has a structure with less steps than that according to the prior art. The semiconductor according to this invention is, therefore, flatter than that according to the prior art.

In the above embodiment, the conductive plug 61 which is not connect to the lower wiring 7 is mainly made of tungsten, and the conductive film for the lower wiring 7 is made of aluminum. Materials of the conductive films for the conductive plug 61 and the lower wiring 7 are, however, not limited to these.

For example, when the conductive film for the lower wiring 7 is mainly made of aluminum and the conductive plug 61 is also made of aluminum, the conductive plug 61 can be readily etched with an etching gas for forming the lower wiring 7. In such a case, i.e., when the conductive plug 61 is made of a material susceptible to etching with an etching gas for forming the lower wiring 7, the process of this invention, in which the upper surface of the conductive plug 61 is protected from the etching gas by providing the coating 8, is particularly effective.

The above adjacent conductive layers in the above embodiment is the gate electrode formed near the surface of

the semiconductor substrate and the source-drain region formed on the surface of the semiconductor substrate. This invention may be, however, applied to a semiconductor device in which the adjacent conductive layers are formed in a layer, over a semiconductor substrate, separated from the surface of the semiconductor substrate.

INDUSTRIAL APPLICABILITY

As described above, according to the process of this invention, a semiconductor device with a shared contact structure without interconnection of wiring over a conductive plug connecting adjacent conductive layers can be prepared by a process which does not cause damages in the conductive plug, with a reduced number of steps compared with the prior art.

There may be, therefore, provided a semiconductor device in which interconnection between adjacent conductive layers are ensured by the conductive plug with the shared contact structure, with a reduced cost compared with that according to the prior art.

In the semiconductor device of this invention or the semiconductor device prepared by the process of this invention, interconnection between adjacent conductive layers are ensured by the conductive plug with the shared contact structure.

CLAIMS

1. A semiconductor device wherein adjacent conductive layers are interconnected via a conductive plug in a single contact hole formed in an interlayer dielectric, a wiring layer is formed just over said interlayer dielectric, and the upper surface of said conductive plug which is not connected to the wiring layer is covered by a conductive coating isolated from said wiring layer.

2. The semiconductor device according to claim 1 wherein said coating is formed by etching the conductive film for said wiring layer, simultaneously with the wiring layer.

3. The semiconductor device according to claim 1 wherein said conductive plug is mainly made of tungsten, and said coating is mainly made of aluminum.

4. The semiconductor device according to claim 1 wherein the whole upper surface of said coating is covered by an insulating film.

5. The semiconductor device according to claim 1 wherein the conductive plug covered by said coating interconnects a gate electrode in an MOS type transistor with an adjacent source-drain region.

6. A process for manufacturing a semiconductor device comprising: a contact hole forming step for forming an interlayer dielectric on a semiconductor substrate including an area where adjacent conductive layers are formed and then a contact hole is formed such that the upper surfaces of said both conductive layers are exposed in the interlayer

dielectric; a conductive plug forming step for forming a conductive plug in the contact hole; a conductive film forming step for forming a conductive film over said interlayer dielectric; and a wiring layer forming step for forming a wiring layer by etching said conductive film, characterized in that

in said conductive film forming step, the conductive film is formed just over said conductive plug and said interlayer dielectric, and

in said wiring layer forming step, a coating isolated from the wiring layer is formed, by etching said conductive film, over said conductive plug which is not connected to said wiring layer, simultaneously with forming the wiring layer.

7. The process according to claim 6 wherein said conductive plug is mainly made of tungsten and said coating is mainly made of aluminum.

8. The process according to claim 6 wherein the whole upper surface of said coating is covered by an insulating film.

9. A process for manufacturing a semiconductor device comprising:

an element forming step for forming a gate electrode and a source-drain region of an MOS type transistor on a semiconductor substrate;

a first interlayer dielectric forming step for forming a first interlayer dielectric on the substrate after said element forming step;

a contact hole forming step for forming a contact hole in said first interlayer dielectric such that the upper

surfaces of the gate electrode and the adjacent source-drain region are exposed;

a conductive plug forming step for forming a conductive plug in said contact hole;

a conductive film forming step for forming a conductive film over said first interlayer dielectric; and

a wiring layer forming step for forming a wiring layer by etching said conductive film, characterized in that

in said conductive film forming step, the conductive film is formed just over said conductive plug and said first interlayer dielectric;

in said wiring layer forming step, a coating isolated from the wiring layer is formed, by etching said conductive film, over said conductive plug which is not connected to said wiring layer, simultaneously with forming the wiring layer; and

after said wiring layer forming step, a second interlayer dielectric is formed just over said wiring layer and the coating.