What is claimed is:

1. A method of forming a field effect transistor, comprising:

forming masking material over semiconductive material of a substrate;

forming a trench through the masking material and into the semiconductive material;

forming gate dielectric material within the trench in the semiconductive material;

depositing gate material within the trench in the masking material and within the trench in the semiconductive material over the gate dielectric material;

recessing the gate material to have a planar outermost surface received within the trench in the masking material, the planar outermost surface spanning completely across the trench in the masking material; and

forming source/drain regions.

2. The method of claim 1 wherein the depositing of the gate material at least fills the trench in the masking material and the trench in the semiconductive material with the gate material.

3. The method of claim 1 wherein the depositing of the gate material overfills the trench in the masking material and the trench in the semiconductive material with the gate material.

4. The method of claim 1 comprising removing at least a majority of the masking material after depositing the gate material.

5. The method of claim 1 being void of photolithographic patterning of the gate material after its deposition.

6. The method of claim 1 wherein depositing the gate material covers the masking material with the gate material, and comprising removing the gate material selectively relative to and exposing the masking material effective to isolate the gate material within the trench in the masking material and the trench in the semiconductive material.

7. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate;

forming array circuitry trenches through the masking material and into the semiconductive material;

depositing array gate material within the array circuitry trenches in the masking material and within the array circuitry trenches in the semiconductive material;

after depositing the array gate material, forming peripheral circuitry trenches through the masking material;

depositing peripheral circuitry gate material within the peripheral circuitry trenches within the masking material;

the array circuitry trenches being formed using a masking step, and further comprising forming grounded gate trenches through the masking material in the array in the same masking step in which the array circuitry trenches are formed, the grounded gate trenches being formed into trench isolation material received within the substrate semiconductive material.

8. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate;

forming array circuitry trenches through the masking material and into the semiconductive material;

depositing array gate material within the array circuitry trenches in the masking material and within the array circuitry trenches in the semiconductive material;

after depositing the array gate material, forming peripheral circuitry trenches through the masking material;

depositing peripheral circuitry gate material within the peripheral circuitry trenches within the masking material;

the peripheral circuitry trenches being formed using a masking step, and further comprising forming grounded gate trenches through the masking material in the array in the same masking step in which the peripheral circuitry trenches are formed, the grounded gate trenches being formed into trench isolation material received within the substrate semiconductive material.

9. A method of forming a field effect transistor, comprising:

forming masking material over semiconductive material of a substrate, the masking material having a thickness expanse over the semiconductive material;

forming a trench through the masking material and into the semiconductive material;

forming gate dielectric material within the trench in the semiconductive material;

depositing gate material within the trench in the masking material and within the trench in the semiconductive material over the gate dielectric material;

recessing the gate material to have an outermost surface spanning completely across the trench in the masking material and that is everywhere received within the trench within the thickness expanse of the masking material and everywhere outward of the semiconductive material into which the trench was formed; and

forming source/drain regions.

10. The method of claim 9 comprising removing at least a majority of the masking material after the recessing.

11. A method of forming a field effect transistor, comprising:

forming masking material over semiconductive material of a substrate;

forming a trench through the masking material and into the semiconductive material;

forming gate dielectric material within the trench in the semiconductive material;

providing gate material within the trench in the masking material and within the trench in the semiconductive material over the gate dielectric material;

exposing sidewalls of the gate material outward of the semiconductive material;

forming insulative material over the sidewalls of the gate material outward of the semiconductive material;

anisotropically etching the insulative material to form insulative sidewall spacers over the sidewalls of the gate material outward of the semiconductive material; and

forming source/drain regions.

12. The method of claim 11 comprising forming the gate material to comprise higher electrically conductive material received over lower electrically conductive material, said exposing of sidewalls of the gate material only being of sidewalls of the higher electrically conductive material.

13. The method of claim 11 comprising forming the gate material to comprise higher electrically conductive material received over lower electrically conductive material, the anisotropically etched sidewall spacers being formed over sidewalls of the higher electrically conductive material.

14. The method of claim 13 wherein the anisotropically etched sidewall spacers are not formed over sidewalls of the lower electrically conductive material.

15. The method of claim 11 wherein the exposing comprises removing only some of the masking material.

16. The method of claim 15 wherein the removing is of an outer layer of one composition selectively relative to an immediately adjacent inner layer of different composition from the one.

17. The method of claim 11 comprising capping the gate material with insulating material prior to said exposing.

18. The method of claim 17 comprising forming the anisotropically etched sidewall spacers over sidewalls of the insulating material.

19. The method of claim 11 comprising:

forming the gate material to comprise higher electrically conductive material received over lower electrically conductive material, the anisotropically etched sidewall spacers being formed over sidewalls of the higher electrically conductive material;

capping the gate material with insulating material prior to said exposing; and

forming the anisotropically etched sidewall spacers over sidewalls of the insulating material.

20. The method of claim 11 wherein the anisotropically etched sidewall spacers are formed outward of a portion of the masking material.

21. The method of claim 11 wherein the anisotropically etched sidewall spacers are formed outward of a portion of the masking material that remains as part of a finished construction of integrated circuitry incorporating the field effect transistor.

22. The method of claim 11 wherein the anisotropically etched sidewall spacers are formed outward of an insulating layer received elevationally atop the semiconductive material.

23. A method of forming a field effect transistor, comprising:

providing gate material within and projecting outwardly of a trench in semiconductive material, the projecting gate material comprising opposing sidewalls outward of the semiconductive material;

providing gate dielectric over the gate material that is within the semiconductive material;

forming insulative material over the sidewalls of the gate material outward of the semiconductive material;

anisotropically etching the insulative material to form insulative sidewall spacers over the sidewalls of the gate material outward of the semiconductive material; and

forming source/drain regions.

24. The method of claim 23 comprising capping the gate material with insulating material prior to said etching.

25. The method of claim 24 comprising forming the anisotropically etched sidewall spacers over sidewalls of the insulating material.

26. The method of claim 23 wherein the anisotropically etched sidewall spacers are formed outward of an insulating layer received elevationally atop the semiconductive material.

27. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate;

in a first masking step, forming array circuitry trenches through the masking material and into the semiconductive material and forming a first peripheral circuitry trench through the masking material;

depositing first gate material within the array circuitry trenches and the first peripheral circuitry trench;

in a second masking step, forming a grounded gate trench through the first gate material and the masking material within array area and forming a second peripheral circuitry trench through the first gate material and the masking material within area peripheral to the array area; and

depositing second gate material within the grounded gate trench and within the second peripheral circuitry trench.

28. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate;

in a first masking step, forming array circuitry trenches through the masking material and into the semiconductive material;

depositing first gate material within the array circuitry trenches;

in a second masking step, forming a grounded gate trench through the first gate material and the masking material within array area and forming a first peripheral circuitry trench through the first gate material and the masking material within area peripheral to the array area;

depositing second gate material within the grounded gate trench and within the first peripheral circuitry trench;

in a third masking step, forming a second peripheral circuitry trench through the second gate material and through the first gate material within the peripheral area; and

depositing third gate material within the second peripheral circuitry trench.

29. The method of claim 28 wherein no trench is formed in the peripheral area using the first masking step.

The invention claimed is:

1. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate;

forming array circuitry trenches through the masking material and into the semiconductive material;

depositing array gate material within the array circuitry trenches in the masking material and within the array circuitry trenches in the semiconductive material;

after depositing the array gate material, forming peripheral circuitry trenches through the masking material;

depositing peripheral circuitry gate material within the peripheral circuitry trenches within the masking material;

the array circuitry trenches being formed using a masking step, and further comprising forming grounded gate trenches through the masking material in the array in the same masking step in which the array circuitry trenches are formed, the grounded gate trenches being formed into trench isolation material received within the substrate semiconductive material.

2. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate;

forming array circuitry trenches through the masking material and into the semiconductive material;

depositing array gate material within the array circuitry trenches in the masking material and within the array circuitry trenches in the semiconductive material;

after depositing the array gate material, forming peripheral circuitry trenches through the masking material;

depositing peripheral circuitry gate material within the peripheral circuitry trenches within the masking material;

the peripheral circuitry trenches being formed using a masking step, and further comprising forming grounded gate trenches through the masking material in the array in the same masking step in which the peripheral circuitry trenches are formed, the grounded gate trenches being formed into trench isolation material received within the substrate semiconductive material.

3. A method of forming a field effect transistor, comprising:

forming masking material over semiconductive material of a substrate;

forming a trench through the masking material and into the semiconductive material;

forming gate dielectric material within the trench in the semiconductive material;

providing gate material within the trench in the masking material and within the trench in the semiconductive material over the gate dielectric material;

exposing sidewalls of the gate material outward of the semiconductive material;

forming insulative material over the sidewalls of the gate material outward of the semiconductive material;

anisotropically etching the insulative material to form insulative sidewall spacers over the sidewalls of the gate material outward of the semiconductive material;

forming source/drain regions; and

forming the gate material to comprise higher electrically conductive material received over lower electrically conductive material, said exposing of sidewalls of the gate material only being of sidewalls of the higher electrically conductive material.

4. A method of forming a field effect transistor, comprising:

forming masking material over semiconductive material of a substrate;

forming a trench through the masking material and into the semiconductive material;

forming gate dielectric material within the trench in the semiconductive material;

providing gate material within the trench in the masking material and within the trench in the semiconductive material over the gate dielectric material;

exposing sidewalls of the gate material outward of the semiconductive material;

forming insulative material over the sidewalls of the gate material outward of the semiconductive material;

anisotropically etching the insulative material to form insulative sidewall spacers over the sidewalls of the gate material outward of the semiconductive material;

forming source/drain regions; and

forming the gate material to comprise higher electrically conductive material received over lower electrically conductive material, the anisotropically etched sidewall spacers being formed over sidewalls of the higher electrically conductive material.

5. The method of claim 4 wherein the anisotropically etched sidewall spacers are not formed over sidewalls of the lower electrically conductive material.

6. A method of forming a field effect transistor, comprising:

forming masking material over semiconductive material of a substrate;

forming a trench through the masking material and into the semiconductive material; forming gate dielectric material within the trench in the semiconductive material;

providing gate material within the trench in the masking material and within the trench in the semiconductive material over the gate dielectric material;

exposing sidewalls of the gate material outward of the semiconductive material;

forming insulative material over the sidewalls of the gate material outward of the semiconductive material;

anisotropically etching the insulative material to form insulative sidewall spacers over the sidewalls of the gate material outward of the semiconductive material;

forming source/drain regions;

forming the gate material to comprise higher electrically conductive material received over lower electrically conductive material,

the anisotropically etched sidewall spacers being formed over sidewalls of the higher electrically conductive material;

capping the gate material with insulating material prior to said exposing; and

forming the anisotropically etched sidewall spacers over sidewalls of the insulating material.

7. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate;

in a first masking step, forming array circuitry trenches through the masking material and into the semiconductive material and forming a first peripheral circuitry trench through the masking material;

depositing first gate material within the array circuitry trenches and the first peripheral circuitry trench;

in a second masking step, forming a grounded gate trench through the first gate material and the masking material within array area and forming a second peripheral circuitry trench through the first gate material and the masking material within area peripheral to the array area; and

depositing second gate material within the grounded gate trench and within the second peripheral circuitry trench.

8. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate;

in a first masking step, forming array circuitry trenches through the masking material and into the semiconductive material;

depositing first gate material within the array circuitry trenches;

in a second masking step, forming a grounded gate trench through the first gate material and the masking material within array area and forming a first peripheral circuitry trench through the first gate material and the masking material within area peripheral to the array area;

depositing second gate material within the grounded gate trench and within the first peripheral circuitry trench;

in a third masking step, forming a second peripheral circuitry trench through the second gate material and through the first gate material within the peripheral area; and

depositing third gate material within the second peripheral circuitry trench.

9. The method of claim 8 wherein no trench is formed in the peripheral area using the first masking step.