ABSTRACT

A METHOD TO AVOID COPPER CONTAMINATION DURING COPPER ETCHING AND CMP

In accordance with the objects of this invention a new method to prevent copper contamination of the intermetal dielectric layer during etching, CMP, or post-etching and post-CMP cleaning by forming a dielectric cap for isolation of the underlying dielectric layer is described. In one embodiment of the invention, a dielectric layer is provided overlying a semiconductor substrate. A dielectric cap layer is deposited overlying the dielectric layer. A via is patterned and filled with a metal layer and planarized. A copper layer is deposited overlying the planarized metal layer and dielectric cap layer. The copper layer is etched to form a copper line wherein the dielectric cap layer prevents copper contamination of the dielectric layer during etching and cleaning. In another embodiment of the invention, a dielectric layer is provided overlying a semiconductor substrate. A dielectric cap layer is deposited overlying the dielectric layer. A dual damascene opening is formed through the dielectric cap layer and the dielectric layer. A copper layer is deposited overlying a barrier metal layer over the dielectric cap layer and filling the dual damascene opening. The copper layer is polished back to leave the copper layer only within the dual damascene opening where the dielectric cap layer prevents copper contamination of the dielectric layer during polishing and cleaning.

(FIGURE 2 IS SUGGESTED FOR PUBLICAITON)