

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a substrate;

a stack comprising a plurality of layers that are vertically stacked on the substrate, each of the plurality of layers comprising semiconductor patterns that extend in a first direction and a first conductive line that is connected to at least one of the semiconductor patterns and extends in a second direction crossing the first direction;

a second conductive line and a third conductive line that extend in a third direction, perpendicular to the first and second directions, to penetrate the stack, wherein the semiconductor patterns comprise a first semiconductor pattern and a second semiconductor pattern that are adjacent and spaced apart from each other in the first direction in a first layer among the plurality of layers, and a third semiconductor pattern, in a second layer among the plurality of layers, that is vertically overlapped by the first semiconductor pattern in the third direction; and

a gate insulating layer,

wherein the gate insulating layer is between the second conductive line and the first and third semiconductor patterns,

wherein the third conductive line is between, and connected in common to, the first and second semiconductor patterns,

wherein each of the semiconductor patterns comprises a first impurity region, a second impurity region, and a third impurity region,

wherein the first and third impurity regions comprise a first conductivity type, and

wherein the second impurity region comprises a second conductivity type different from the first conductivity type.

2. The semiconductor memory device of claim 1,

wherein the first conductive line is connected to the first impurity region, and

wherein the second conductive line is adjacent the second impurity region.

3. The semiconductor memory device of claim 1 or claim 2,

wherein each of the semiconductor patterns further comprises a fourth impurity region,

wherein the fourth impurity region comprises the second conductivity type, and
wherein the third conductive line is connected to the fourth impurity region.

4. The semiconductor memory device of any one of claims 1 to 3,
wherein the first conductive line is on a top surface of the first semiconductor pattern,
and
wherein a memory cell comprising the first semiconductor pattern comprises a
capacitor-free memory cell.

5. The semiconductor memory device of any one of claims 1 to 4,
wherein the second conductive line comprises a first sub-conductive line and a
second sub-conductive line that extend in the third direction,
wherein each of the first and third semiconductor patterns comprises a first side wall
and a second side wall opposite to the first side wall,
wherein the first sub-conductive line is adjacent the first side wall, and
wherein the second sub-conductive line is adjacent the second side wall.

6. The semiconductor memory device of claim 1 or claim 2,
wherein the semiconductor patterns further comprise a fourth semiconductor pattern
that is adjacent and spaced apart from the first semiconductor pattern in the second direction
in the first layer, and
wherein the semiconductor memory device further comprises a shield line that
extends in the third direction to penetrate the stack between the first and fourth semiconductor
patterns.

7. The semiconductor memory device of any one of claims 1 to 6, wherein the
first and third semiconductor patterns penetrate the second conductive line.

8. A semiconductor memory device comprising:
a substrate;
a stack comprising a plurality of layers that are vertically stacked on the substrate,
each of the plurality of layers comprising first and second semiconductor structures that are
adjacent and spaced apart from each other in a first direction, and a first conductive line that

extends in the first direction to connect to the first and second semiconductor structures;

second conductive lines that extend vertically in a second direction that is perpendicular to the first direction to penetrate the stack and are spaced apart from each other in the first direction, first and second ones of the second conductive lines being adjacent the first and second semiconductor structures, respectively;

a first gate insulating layer between the first semiconductor structure and the first one of the second conductive lines;

a second gate insulating layer between the second semiconductor structure and the second one of the second conductive lines;

third conductive lines that extend vertically in the second direction and are spaced apart from each other in the first direction, first and second ones of the third conductive lines being connected to respective first ends of the first and second semiconductor structures; and

a shield line that extends vertically in the second direction to penetrate the stack between the first and second ones of the second conductive lines,

wherein each of the first and second semiconductor structures comprises a first impurity region, a second impurity region, and a third impurity region,

wherein the first and third impurity regions comprise a first conductivity type, and

wherein the second impurity region comprises a second conductivity type different from the first conductivity type.

9. The semiconductor memory device of claim 8,

wherein the first conductive line is connected to the first impurity region, and

wherein the second conductive line is adjacent the second impurity region.

10. The semiconductor memory device of claim 9,

wherein each of the first and second semiconductor structures further comprises lightly-doped regions between the first and second impurity regions and between the second and third impurity regions,

wherein the lightly-doped regions comprise the first conductivity type, and

wherein an impurity concentration of the lightly-doped regions is lower than an impurity concentration of the first and third impurity regions.

11. The semiconductor memory device of claim 9 or claim 10,

wherein each of the first and second semiconductor structures further comprises a fourth impurity region adjacent the first end,

wherein the fourth impurity region comprises the second conductivity type, and

wherein the third conductive lines are connected to the fourth impurity region.

12. The semiconductor memory device of any one of claims 8 to 11,
wherein each of the first and second semiconductor structures comprises a second end that is opposite to the first end, and

wherein the first conductive line is on respective top surfaces of the first and second semiconductor structures and adjacent the second end.

13. The semiconductor memory device of any one of claims 8 to 12,
wherein each of the second conductive lines comprises a first sub-conductive line and a second sub-conductive line that extend vertically in the second direction,

wherein each of the first and second semiconductor structures comprises a first side wall and a second side wall opposite to the first side wall,

wherein the first sub-conductive line is adjacent the first side wall, and

wherein the second sub-conductive line is adjacent the second side wall.

14. The semiconductor memory device of any one of claims 8 to 13, wherein the first and second semiconductor structures penetrate the first and second ones of the second conductive lines, respectively.

15. The semiconductor memory device of any one of claims 8 to 14, further comprising:

a first silicide layer between the first conductive line and each of the first and second semiconductor structures; and

a second silicide layer between the first and second ones of the third conductive lines and the first and second semiconductor structures, respectively.

16. A semiconductor memory device comprising:

a substrate;

a stack comprising a plurality of layers that are vertically stacked on the substrate,

each of the plurality of layers comprising a first insulating layer, a semiconductor layer, and a second insulating layer that are sequentially stacked;

a first conductive line that is in the second insulating layer and extends in a first direction;

a second conductive line and a third conductive line that extend vertically to penetrate the stack; and

a gate insulating layer adjacent the second conductive line,

wherein the semiconductor layer comprises a semiconductor pattern that is overlapped by the first conductive line and extends in a second direction crossing the first direction,

wherein the gate insulating layer is between the second conductive line and the semiconductor pattern,

wherein the third conductive line is connected to a first end of the semiconductor pattern,

wherein the semiconductor pattern comprises a first impurity region, a second impurity region, and a third impurity region,

wherein the first and third impurity regions comprise a first conductivity type, and

wherein the second impurity region comprises a second conductivity type different from the first conductivity type.

17. The semiconductor memory device of claim 16,

wherein the first conductive line is connected to the first impurity region, and

wherein the second conductive line is adjacent the second impurity region.

18. The semiconductor memory device of claim 16 or claim 17,

wherein the semiconductor pattern further comprises a fourth impurity region,

wherein the fourth impurity region comprises the second conductivity type, and

wherein the third conductive line is connected to the fourth impurity region.

19. The semiconductor memory device of any one of claims 16 to 18,

wherein the semiconductor pattern comprises a second end that is opposite to the first end, and

wherein the first conductive line is on a top surface of the semiconductor pattern and

adjacent the second end.

20. The semiconductor memory device of any one of claims 16 to 19,
wherein the second conductive line comprises a first sub-conductive line and a
second sub-conductive line that extend vertically,
wherein the semiconductor pattern comprises a first side wall and a second side wall
opposite to the first side wall,
wherein the first sub-conductive line is adjacent the first side wall, and
wherein the second sub-conductive line is adjacent the second side wall.