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HIGH BANDWIDTH REED-SOLOMON ENCODING, DECODING AND ERROR CORRECTING CIRCUIT

ABSTRACT OF THE DISCLOSURE

A VLSI circuit that implements a symmetric Reed-Solomon error correcting code for correcting up to 32 symbol errors per code word in real time. Extensive use of data pipelining and novel solutions to the Berlekamp-Massey algorithm without supplementary software or heavily iterative hardware calculations provide a high bandwidth, low latency implementation of the Reed-Solomon code with low data overhead and low hardware cost.

This Sheet Has Been Replaced

