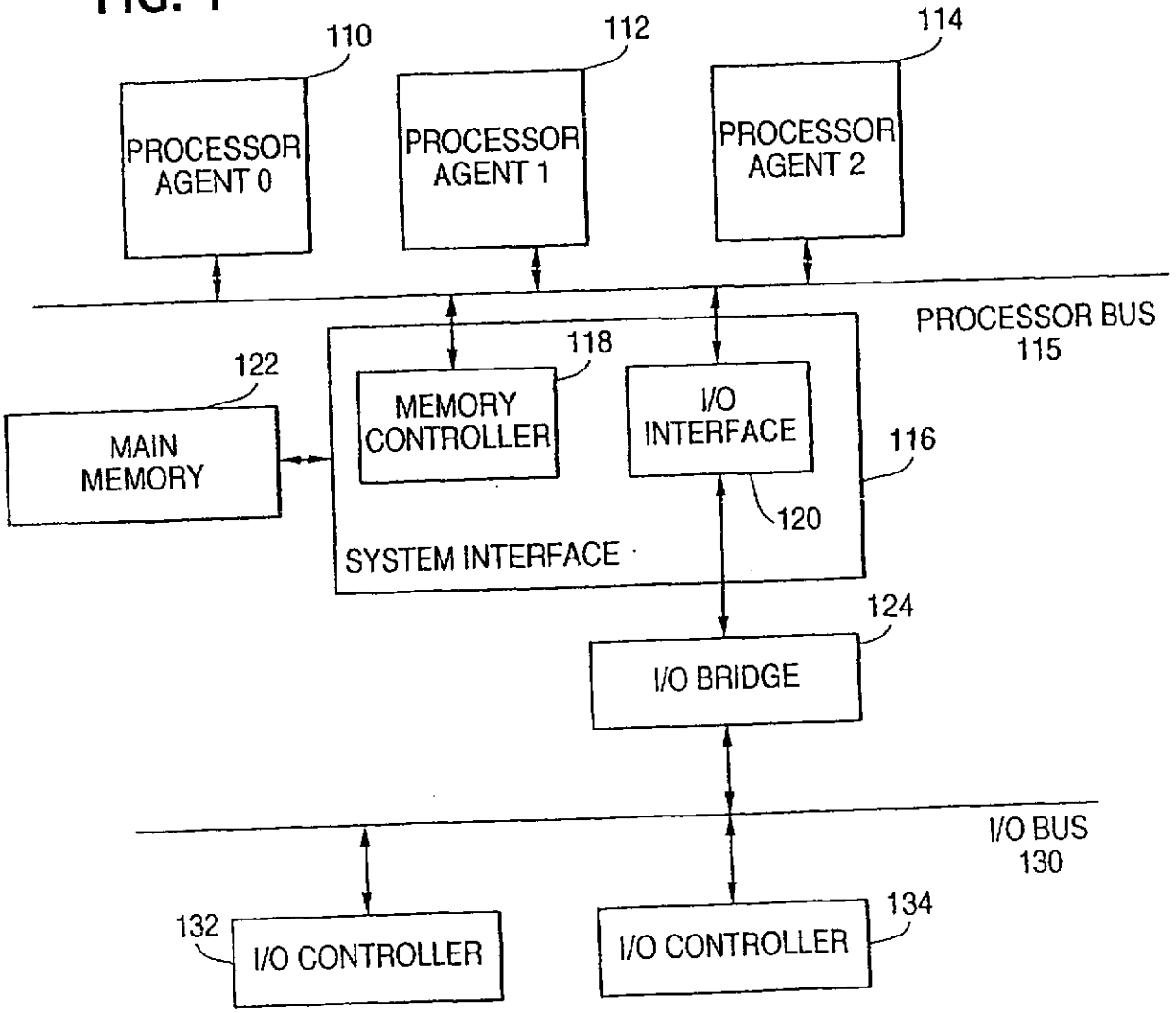
FIG. 1



COMPUTER 100

FIG. 2

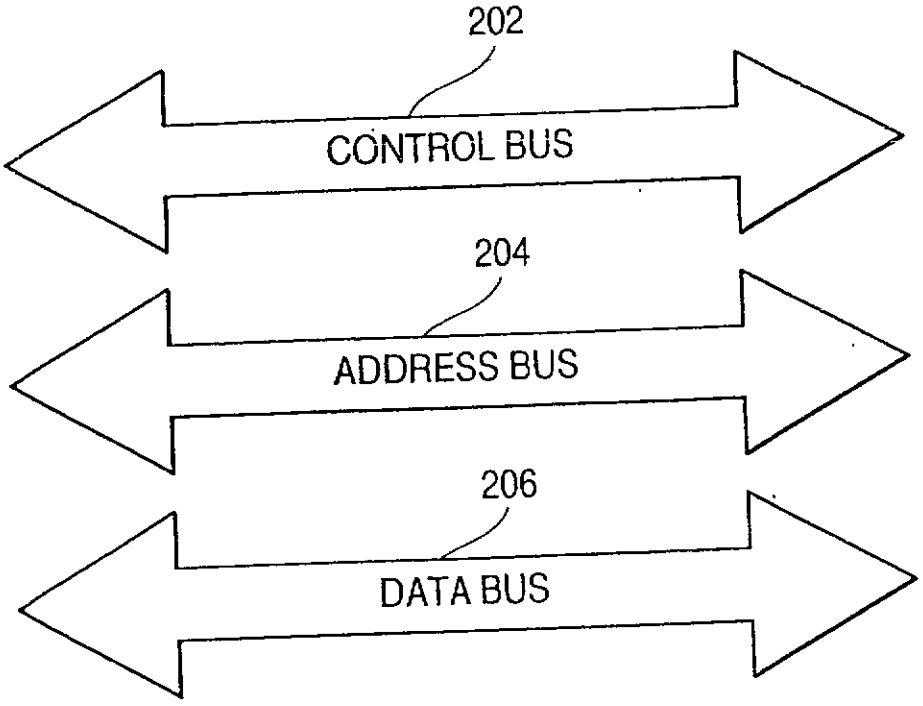
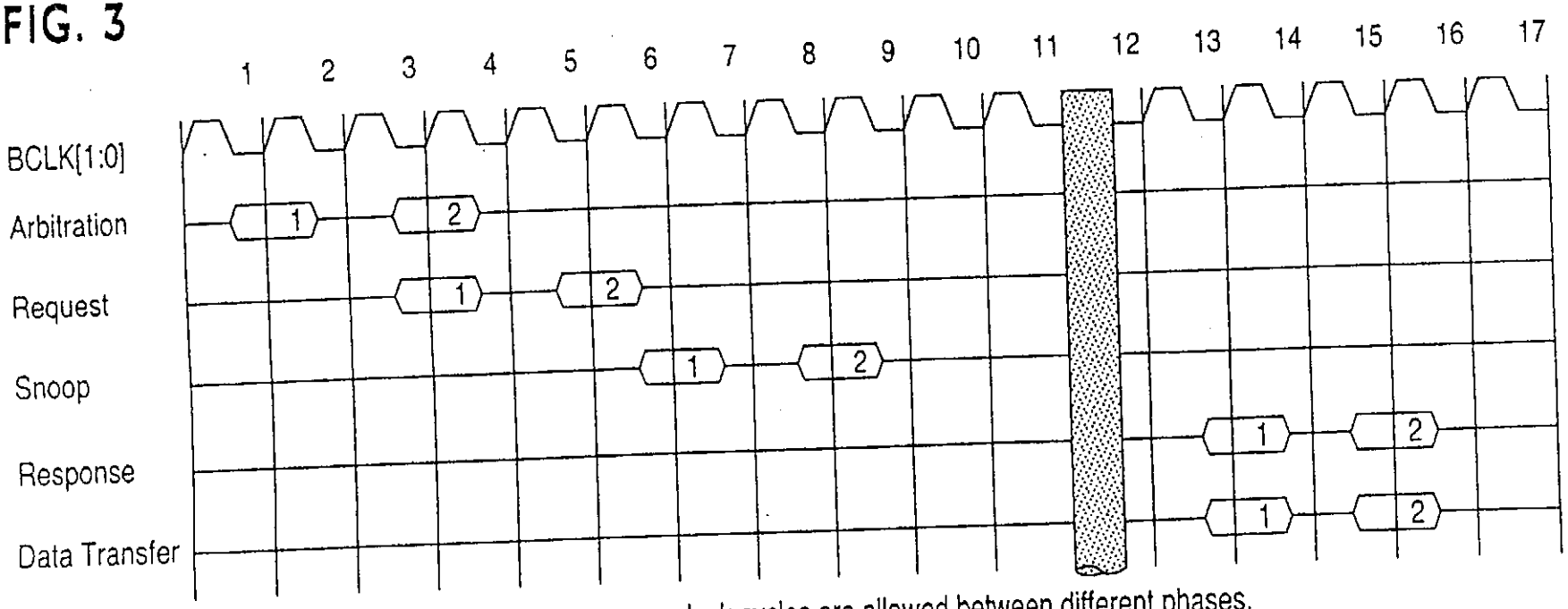

202
CONTROL BUS
204
ADDRESS BUS
206
DATA BUS
PROCESSOR BUS
115

FIG. 3



* NOTE: The shaded vertical bar indicates one or more clock cycles are allowed between different phases.

FIG. 4

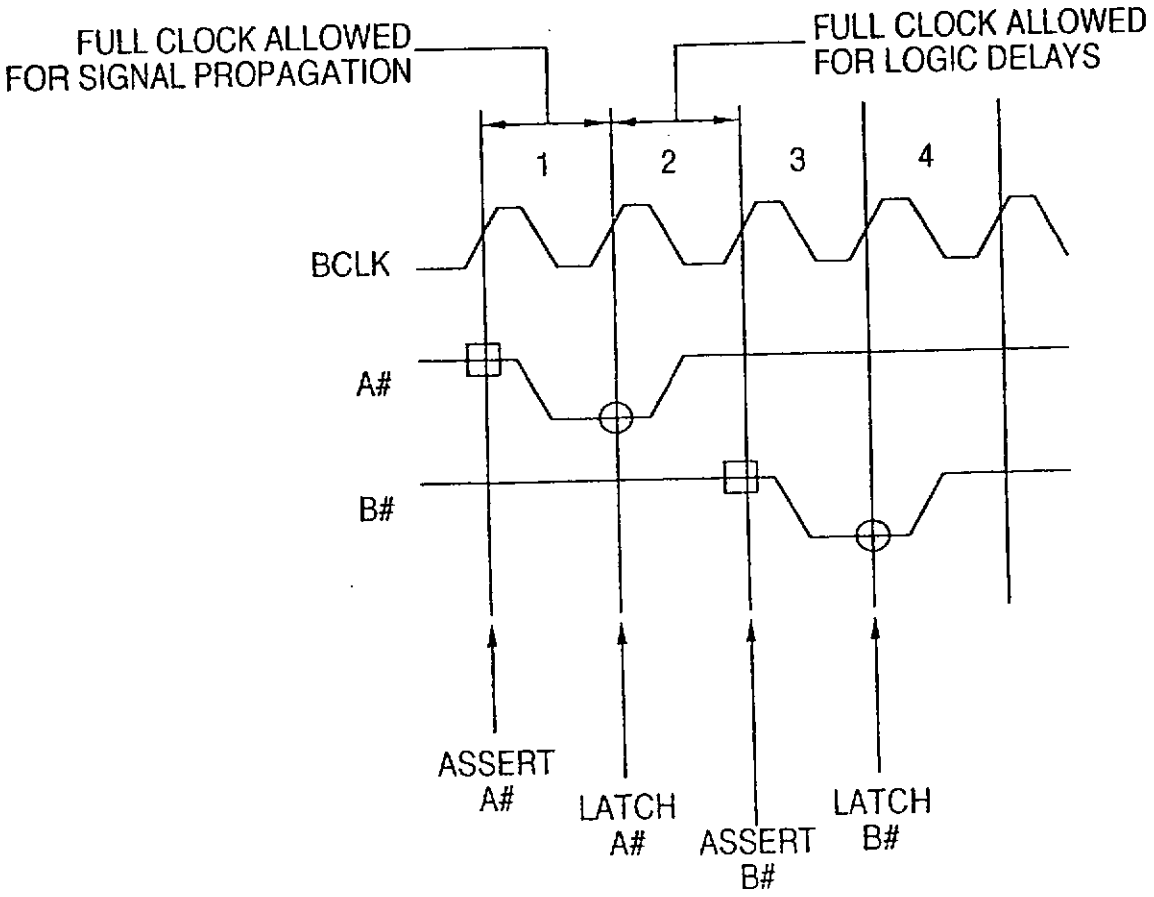

FULL CLOCK ALLOWED
FOR SIGNAL PROPAGATION
FULL CLOCK ALLOWED
FOR LOGIC DELAYS
1
2
3
4
BCLK
A#
B#
ASSERT
A#
LATCH
A#
ASSERT
B#
LATCH
B#

FIG. 5

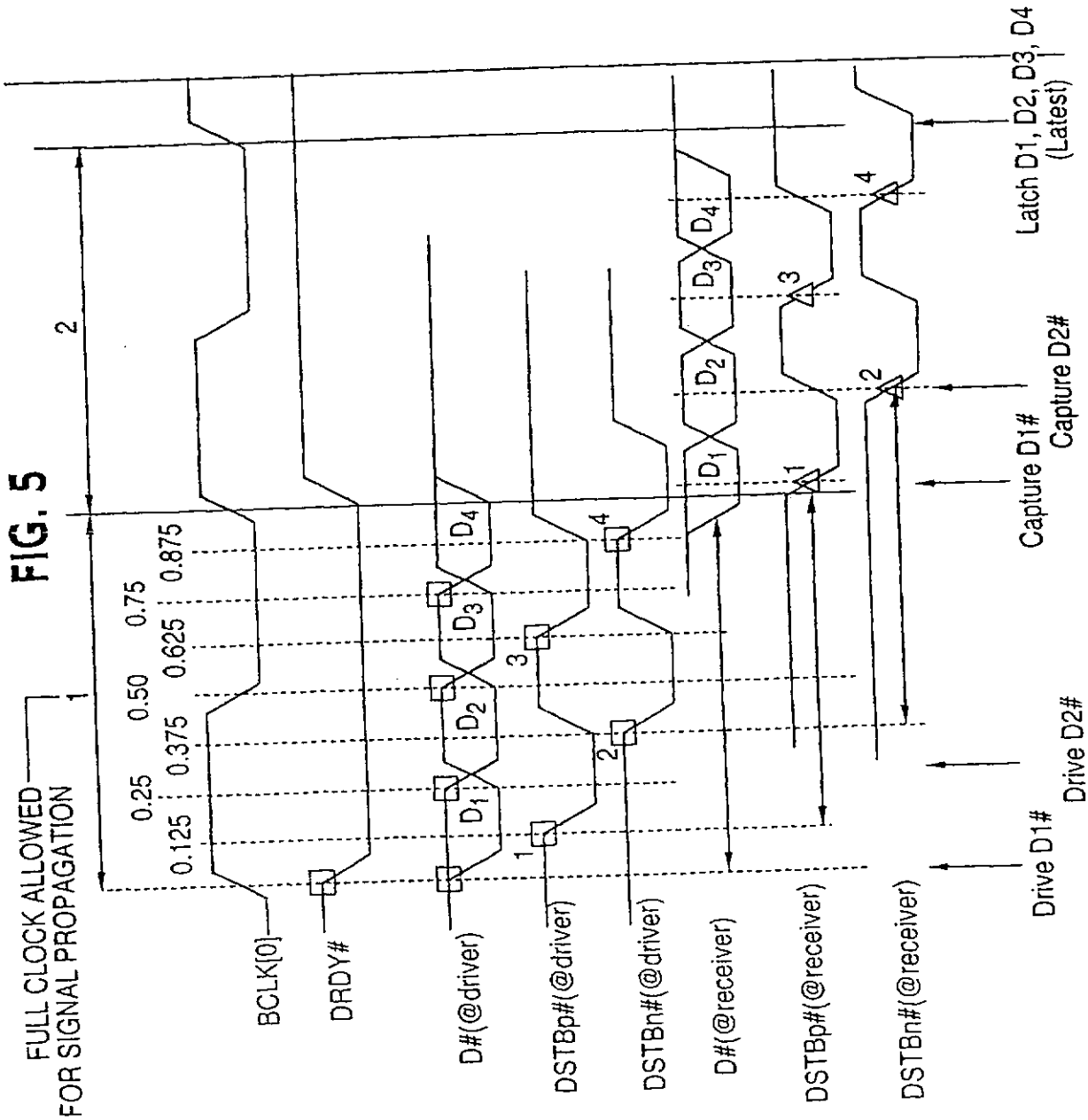

FULL CLOCK ALLOWED
FOR SIGNAL PROPAGATION
1
2
0.125
0.25
0.375
0.50
0.625
0.75
0.875
BCLK[0]
DRDY#
D#(@driver)
DSTBp#(@driver)
DSTBn#(@driver)
D#(@receiver)
DSTBp#(@receiver)
DSTBn#(@receiver)
D1
D2
D3
D4
Drive D1#
Drive D2#
Capture D1#
Capture D2#
Latch D1, D2, D3, D4
(Latest)

FIG. 6

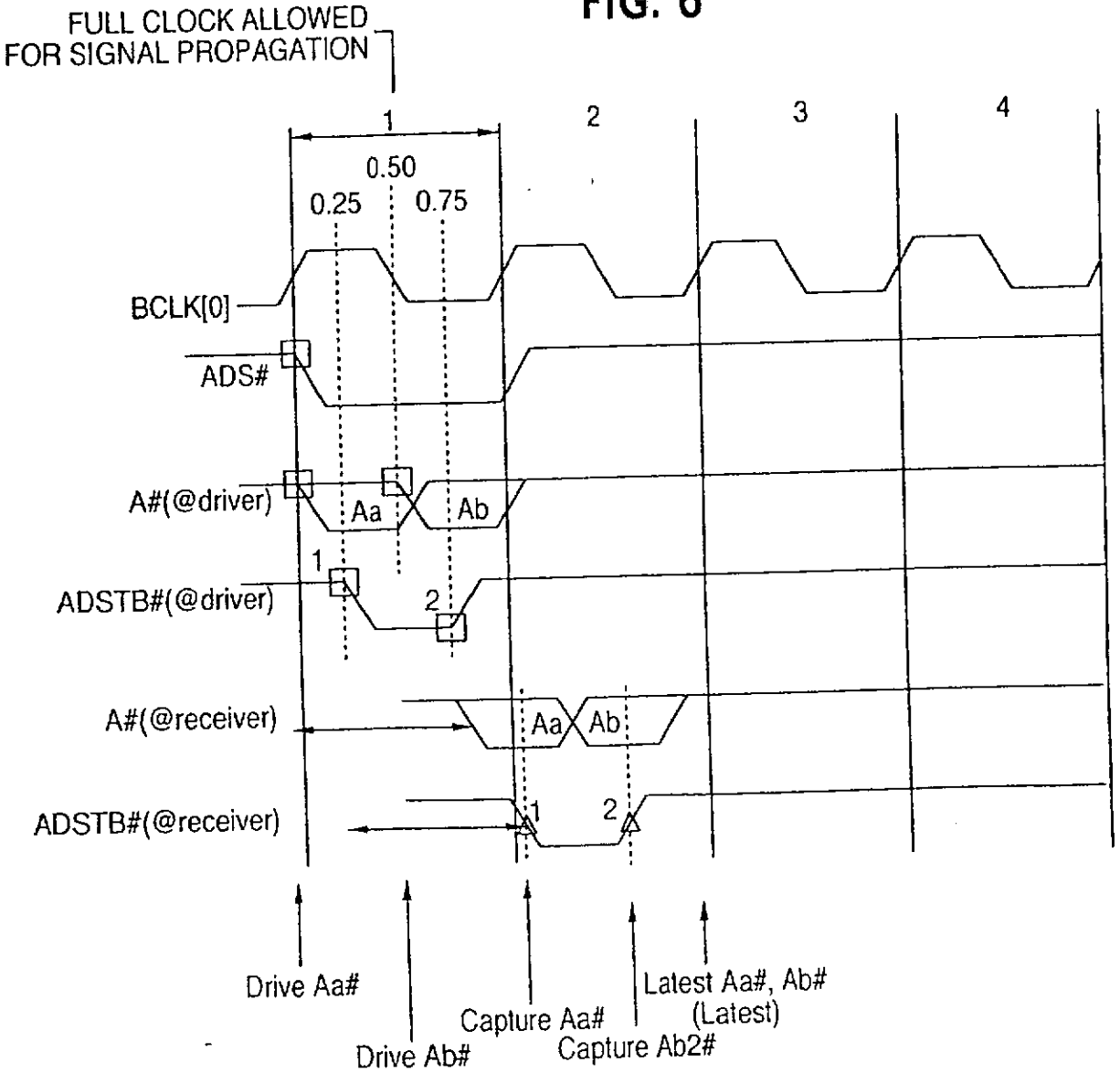
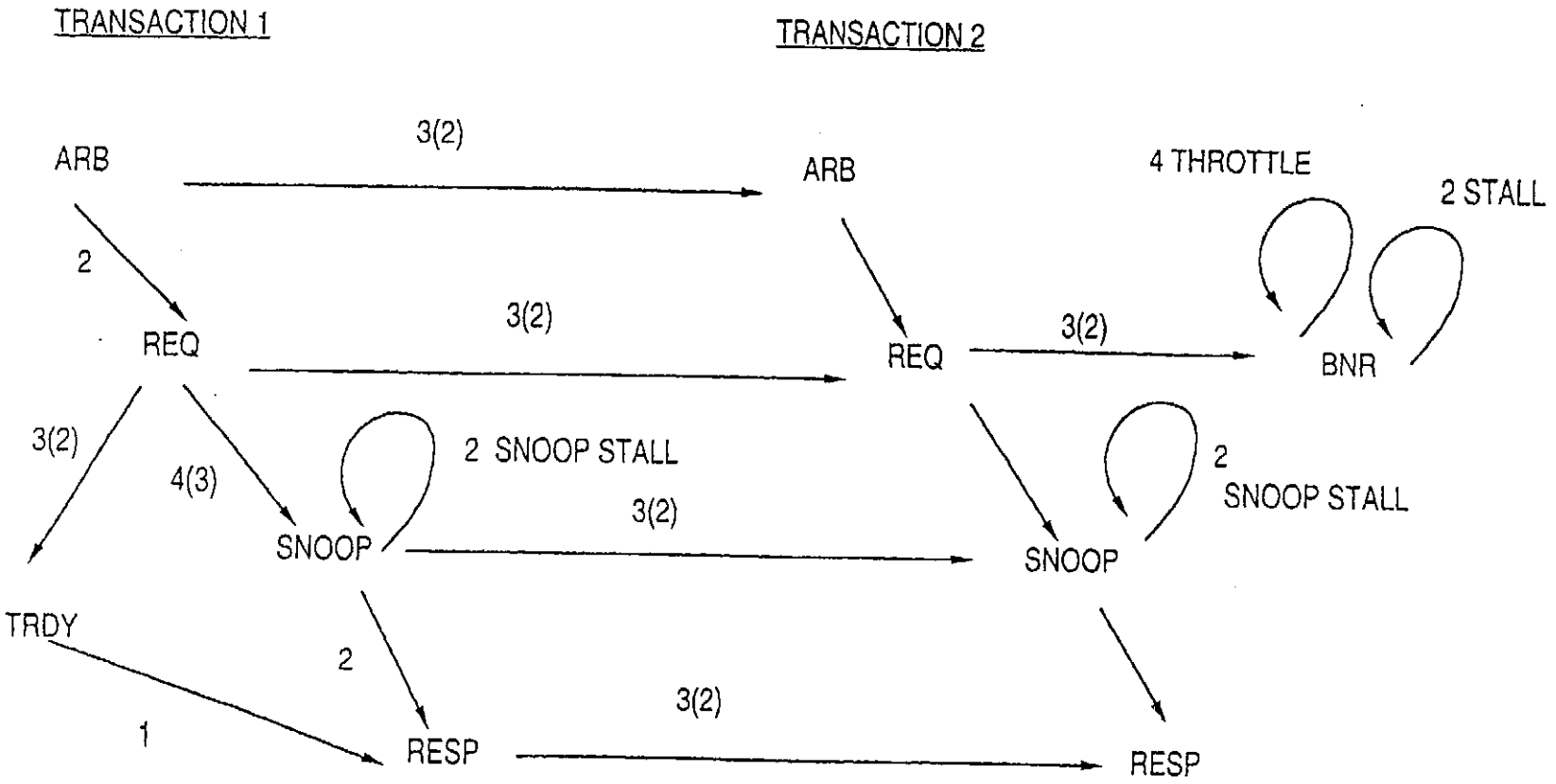

FULL CLOCK ALLOWED
FOR SIGNAL PROPAGATION
1
2
3
4
0.50
0.25
0.75
BCLK[0]
ADS#
A#(@driver)
Aa
Ab
1
2
ADSTB#(@driver)
A#(@receiver)
Aa
Ab
1
2
ADSTB#(@receiver)
Drive Aa#
Drive Ab#
Capture Aa#
Capture Ab2#
Latest Aa#, Ab#
(Latest)

FIG. 7


TRANSACTION 1
TRANSACTION 2
ARB
3(2)
ARB
4 THROTTLE
2 STALL
2
REQ
3(2)
REQ
3(2)
BNR
3(2)
4(3)
2 SNOOP STALL
3(2)
SNOOP
SNOOP
2
SNOOP STALL
TRDY
2
3(2)
1
RESP
RESP

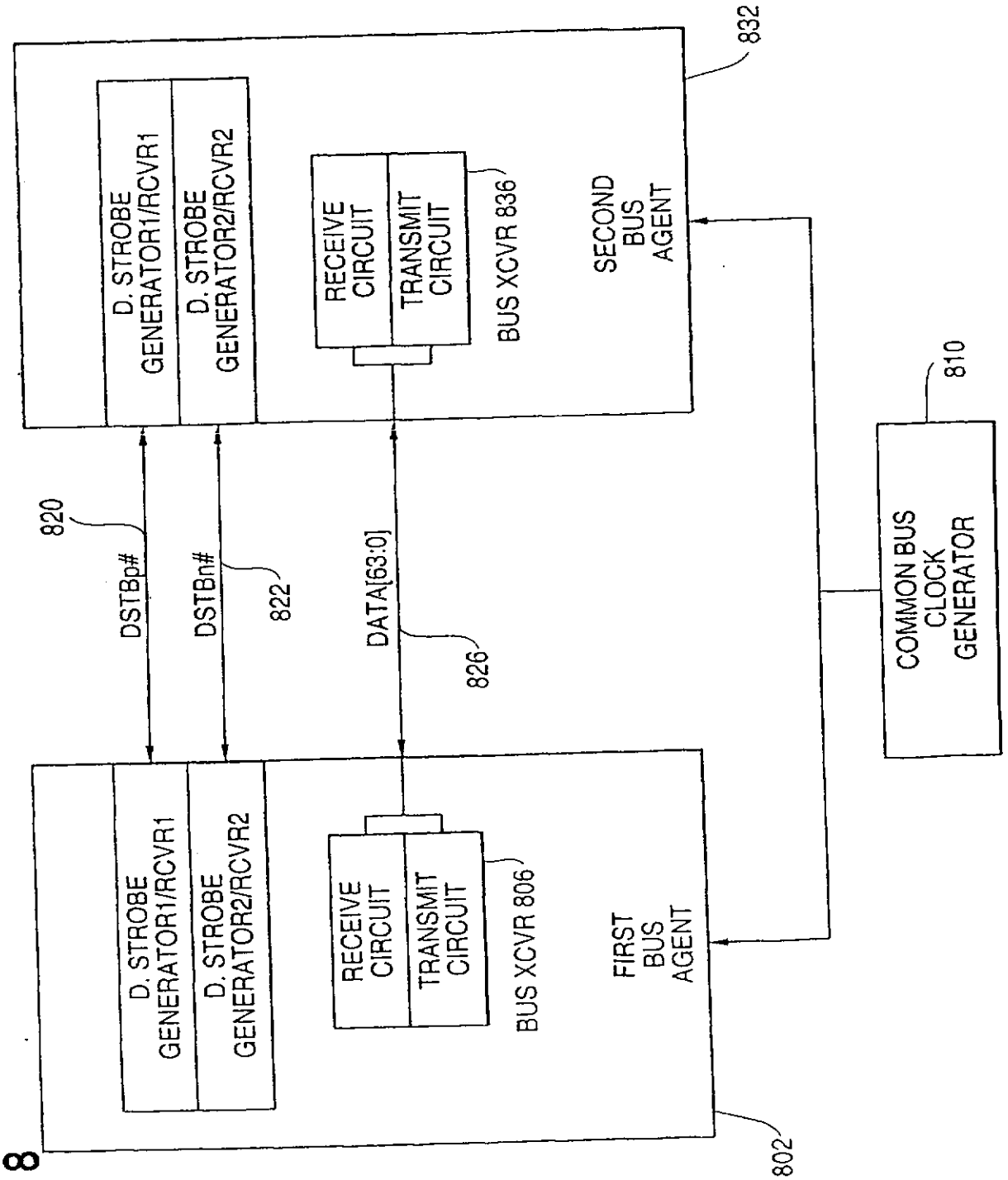

832
D. STROBE GENERATOR1/RCVR1
D. STROBE GENERATOR2/RCVR2
RECEIVE CIRCUIT
TRANSMIT CIRCUIT
BUS XCVR 836
SECOND BUS AGENT
820
DSTBp#
DSTBn#
822
DATA[63:0]
826
COMMON BUS CLOCK GENERATOR
810
D. STROBE GENERATOR1/RCVR1
D. STROBE GENERATOR2/RCVR2
RECEIVE CIRCUIT
TRANSMIT CIRCUIT
BUS XCVR 806
FIRST BUS AGENT
802

FIG. 8

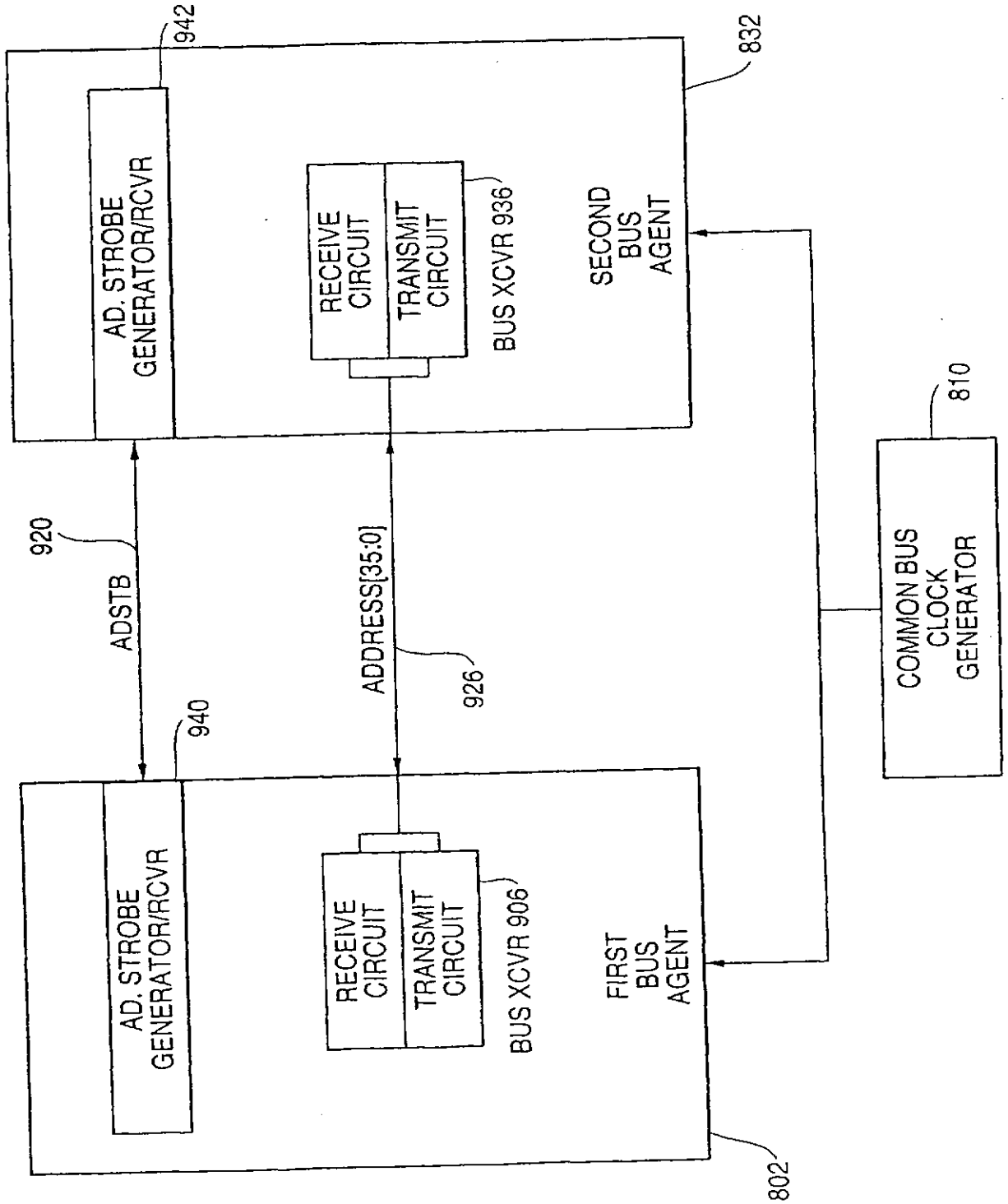

942
832
AD. STROBE GENERATOR/RCVR
RECEIVE CIRCUIT
TRANSMIT CIRCUIT
BUS XCVR 936
SECOND BUS AGENT
920
ADSTB
ADDRESS[35:0]
926
940
AD. STROBE GENERATOR/RCVR
RECEIVE CIRCUIT
TRANSMIT CIRCUIT
BUS XCVR 906
FIRST BUS AGENT
802
COMMON BUS CLOCK GENERATOR
810

FIG. 9