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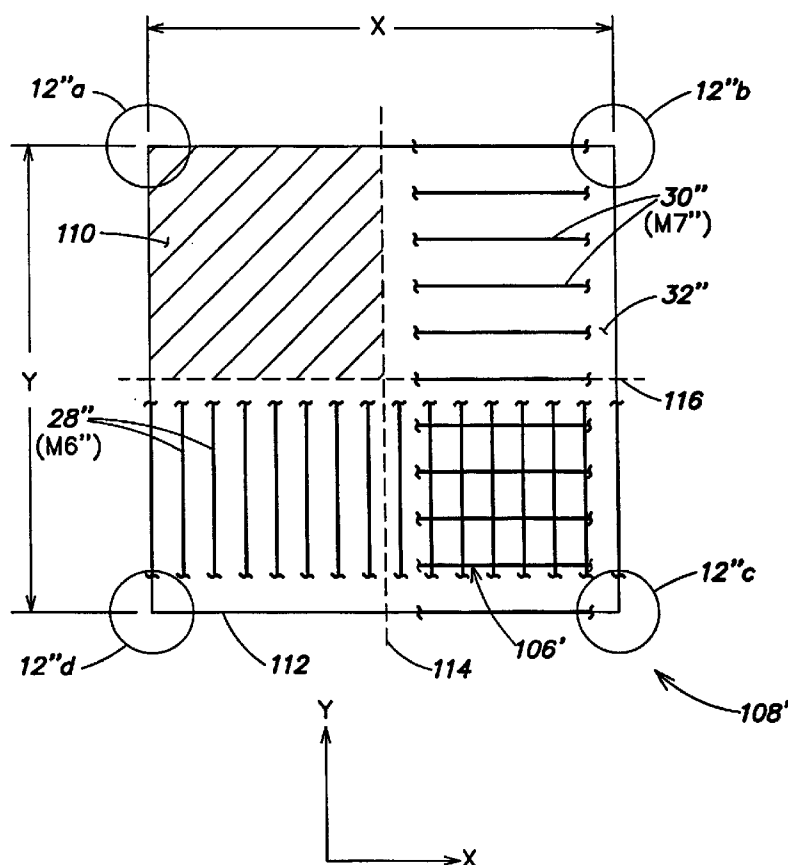
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[Continued on next page]

(54) Title: INTEGRATED CIRCUIT BUS GRID HAVING WIRES WITH PRE-SELECTED VARIABLE WIDTHS



(57) Abstract: An electrical bus grid (108) for an application specific integrated circuit (ASIC) chip (102). The bus grid is generally formed by mutually orthogonal wires (28', 30') contained within two metal layer (M6', M7'). The bus grid is located within each of a plurality of contiguous rectangular regions (32'), which are defined by electrical contacts (12'). Due to the regular pattern of the electrical contacts, the bus grids within the contiguous rectangular regions are identical to one another, such that the bus grid forms a repeatable pattern. The widths of the wires in each of the two metal layers vary depending upon the magnitude of the current carried by the corresponding wire. The magnitude of the current in the power bus may be determined by simulation and modeling performed prior to placement of cells (e.g., 18, 20, 22) within the ASIC chip.

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