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APPARATUS AND METHOD FOR DIRECT SILICON CHIP ATTACHMENT TO A LEAD FRAME

TECHNICAL FIELD OF THE INVENTION

The present invention relates in general to the field of high frequency integrated circuit packages and more specifically to an apparatus and method of using a copper layer between the silicon chip and the substrate to provide for increased bonding strength between the substrate and the silicon chip.

BACKGROUND OF THE INVENTION

Without limiting the scope of the invention, its background is described in connection with integrated circuit packages, as an example.

Heretofore, in this field, integrated circuits have been formed on semiconductor wafers. The wafers are separated into individual chips and the individual chips are then handled and packaged. The packaging process is one of the most critical steps in the integrated circuit fabrication process, both from the point of view of cost and of reliability. Specifically, the packaging cost can easily exceed the cost of the integrated circuit chip and the majority of device failures are packaging related.

The integrated circuit must be packaged in a suitable media that will protect it in subsequent manufacturing steps and from the environment of its intended application. Wire bonding and encapsulation are the two main steps in the packaging process. Wire bonding connects the leads from the chip to the terminals of the package. The terminals allow the integrated circuit package to be connected to other components. Following wire bonding, encapsulation is employed to seal the surfaces from

moisture and contamination and to protect the wire bonding and other components from corrosion and mechanical shock.

Conventionally, the packaging of integrated circuits has involved attaching an individual chip to a lead frame, where, following wire bonding and encapsulation, designated parts of the lead frame become the terminals of the package. The packaging of integrated circuits has also involved the placement of chips on a flexible board where, following adhesion of the chip to the surface of the flexible board and wire bonding, an encapsulant is placed over the chip and the adjacent flexible board to seal and protect the chip and other components.

Unfortunately, current methods for attaching silicon chips to substrates, and the encapsulation of these components, have led to various problems, including cracking between the encapsulation material and the integrated circuit components, as well as high failure rates due to the multi-step nature of the process. Cracking and separation of the components has plagued the industry because of differences in the coefficient of thermal expansion of the different components, for example, between the soldering materials at the different interfaces and between metallic and non-metallic components. Cracking and separation are also frequent between the silicon wafer and the

encapsulation materials, usually epoxies, due to the extreme variations in temperature in various environments and between periods of operation and non-operation.

Even after successful encapsulation of a silicon chip in an integrated circuit package, another problem commonly encountered is loss of coplanarity. Once the silicon chip is encapsulated it is typically surface mounted using radiant heat or vapor saturated heating. This process, however, can lead to poor coplanarity between the components due to uneven reflow, leading to integrated circuit failure.

Therefore, a need has arisen for an integrated circuit package and a process for producing an integrated circuit package that solves the problem of separation between a silicon chip and a flexible board. A need has also arisen for an integrated circuit package that protects the chip during subsequent manufacturing and testing steps as well as from the environment of its intended purpose. Further, need has arisen for a smaller, more versatile integrated circuit package made from materials and by methods that lead to increased yield by more closely matching the coefficient of thermal expansion of the materials used in the package.

SUMMARY OF THE INVENTION

The present invention disclosed herein comprises an integrated circuit package and a process for producing an integrated circuit package that protects the silicon chip during manufacturing and testing steps. The integrated circuit package and process disclosed herein protects the components from the environment of its intended purpose using materials and processing that better adheres the silicon chip to the printed circuit board.

The integrated circuit package is produced by placing a layer of a metal, such as copper, between the substrate and the adhesive material on one surface of the integrated circuit. For example, the adhesive material can be placed on either the chip or the substrate.

The substrate has an opening and first and second surfaces. A plurality of routing strips are integral with the substrate and extend into the opening. A plurality of pads are disposed on the first surface, at least one of the pads is electrically connected with at least one of the routing strips. The chip has at least one bonding pad. Wire bonding electrically connecting the bonding pad to at least one of the routing strips. Potting material fills the opening. At least one solder ball is

attached to at least one of the pads disposed on the first surface.

In the method of the present invention, a layer of a conductive metal, such as copper, is disposed on either the chip or the substrate. The method of attaching the chip to the substrate also includes positioning the chip or the substrate in contact with the adhesive layer. The chip can be mounted on a stage where heat is applied to the chip or the substrate. Also, force may be applied to the chip. Alternatively, both heat and force may be applied to the chip and substrate assembly. In one embodiment of the present invention, the temperature applied to the chip is between about 200 °C and 250 °C and may preferably be about 220 °C. In another embodiment of the present invention, the force applied to the chip may be between about 150 and 200 grams and preferably about 175 grams. The force may be applied for between about 2 and 10 seconds and preferably for about 5 seconds.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the features and advantages of the present invention, reference is now made to the detailed description of the invention along with the accompanying figures in which corresponding numerals in the different figures refer to corresponding parts and in which:

Figure 1 is a simplified end cross-sectional view of an integrated circuit package of the present invention; and

Figure 2 is a simplified top view of an integrated circuit package of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

While the making and using of various embodiments of the present invention are discussed in detail below, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention and do not delimit the scope of the invention.

The present invention is related to high frequency integrated circuits using a board-on-chip design that enables a reduction in processing steps during the production of integrated circuit packages. In addition to the improved processing method, the present invention meets the space constraint requirements of modern semiconductors. The principles of the present invention may be incorporated into, for example, a synchronous DRAM (SDRAM) silicon chip. However, the present invention is also applicable to LOGIC, SRAM, EPROM and any other integrated circuit components.

Figure 1 is a simplified cross-sectional view of an integrated circuit package that is generally designated 30. The integrated circuit package 30 comprises a silicon chip 50, which can be, for example, any integrated circuit component such as a

DRAM, an EPROM, an EEPROM, a PROM, a SRAM or a LOGIC chip. An adhesive material 60 is shown in contact with the silicon chip 50. The adhesive material 60 can be, for example, a polyimide tape or liquid adhesive. A metal layer 62 between the printed circuit board 70 and the adhesive layer 60 increases the adherence of the printed circuit board 70 and the silicon chip 50. The metal layer 62 can be a metal such as copper, gold or silver. The printed circuit board 70, can consist of one or more layers, depending on the number of vias and conduits that are deposited along the edge of opening 86. A second metal layer 64 is deposited on the printed circuit board 70

The printed circuit board 70 may be constructed from a material such as FR-4, FR-5 or BT resin. FR-4, which is available from Motorola Inc., U.S.A., is an epoxy resin reinforced with a woven glass cloth. Alternatively, the printed circuit board 70 is an organic substrate such as FR-5 or a BT resin. When selecting the material for printed circuit board 70, one skilled in the art will recognize that four parameters should be considered, namely, thickness, dielectric constant, glass transition temperature and the coefficient of thermal expansion.

Thickness is dependent on the number of layers required and the amount of reinforcement used in a given layer. The reinforcing glass cloth can range in thickness from, for example, 2 mil per sheet (type 106) to about 8 mil per sheet (type 7628). Dielectric constant is determined by a combination of the resin used and the thickness and type of reinforcement used. Standard FR-4 has a dielectric constant of about 4.5. This constant can be reduced to about 3 by replacing the epoxy resin with a cyanate ester resin. The greater the thickness, however, the greater the problems associated with thickness control, rough surfaces, excessive drill reflection and poor resin refill.

The temperature at which a resin changes from a glass-like state into a "rubbery" state is generally designated as T_g. Standard FR-4 is made with a bifunctionally polymerizing epoxy that has a T_g of about 110 °C. Higher T_g temperatures, such as 125-150 °C may be withstood by using a tetrafunctional epoxy. For higher T_g values, in the range of 150 to 200 °C a cyanate ester:epoxy blend can be used. Additionally, polyimides provide for printed circuit boards having a T_g above 250 °C.

The coefficient of thermal expansion for FR-4 is about 16 ppm/°C. A difference in the coefficient of thermal expansion

between the printed circuit board 70 made from FR-4 and the silicon chip 50 can lead to failure of the integrated circuit package 30 during, not only the assembly of the integrated circuit package 30, but also during the use of integrated circuit package 30.

The metal layer 62 is disposed between the adhesive layer 60 and either the silicon chip 50 or the printed circuit board 70. The metal layer 62 increases the bonding strength of the adhesive layer 60 and the silicon chip 50 or the printed circuit board 70. If the metal layer 62 has been previously disposed on either of the integrated circuit components (silicon chip 50 or printed circuit board 70) the adhesion of these components remains a one-step process, allowing for the continued use of present integrated circuit packaging machinery and procedures.

The adhesive material 60 is a polyimide layer that can be deposited on the silicon chip 50 as a liquid adhesive prior to, for example, UV-light fixation. Alternatively, the polyimide adhesive of the adhesive layer 60 may be a tape adhesive or film, for example, a 3 mil adhesive polyamide tape. Alternatively, the silicon chip 50 can be adhered to the printed circuit board 70 with a die bonding film such as HIATTACH-335 (DF-335) manufactured by Hitachi Chemical Company of Tokyo,

Japan. HIATTACH-335 (DF-335) is silver filled thermosetting type resin film for die-attaching.

DF-335 has the following properties

Test	Remarks	Units	DF-335
Appearance	Visual	-	silver film
Solid Content	200°C-2h	wt%	≥96
Ash Content	600°C-1.5h	wt%	40
Ash Content/ Solid	600°C-1.5h	wt%/solid	42
Thickness	Dial gauge	μm	25
Tensile Strength	R.T.	kgf/mm²	7.1
Tensile Modulus	R.T.	kgf/mm²	271
Die shear strength	4x4mm chip/Ag plated alloy 42	kgf/chip	
R.T.			≥10
250°C			0.9
Peel strength 240°C (after/ 85°C 85%,48h)	8x8mm chip /bare alloy 42	kgf/chip	≥3.0
Tg	TMA, 180°C-1h cured	°C	123
Modulus	Viscoelastic spectrometer	Mpa	1300
Moisture	85°C/85%RH, 48h	wt%	0.1

Other examples of adhesives include thermosetting adhesives, such as epoxies and silicone. Thermoplastic adhesives that are hot-melted, in the form of sheets or as a pressure sensitive adhesive tape may also be used to adhere

silicon chip 50 to the printed circuit board 70. Commonly used are adhesive tapes based on elastomers, silicones or acrylics because of their ease of use and easy incorporation into production.

Referring collectively to Figures 1 and 2, the printed circuit board 70 has routing strips 82 that are electrically connected through vias or conduits to pads 100 located on top surface 92 of printed circuit board 70. It should be understood by one skilled in the art that the terms "top" and "bottom" as well as the terms "side" and "end" are used for illustration purposes only, as the integrated circuit package 30 of the present invention can be assembled and used in a variety of positions and ways. The printed circuit board 70 can include a pair of bus bars 110. The bus bars are electrically connected through vias to one or more of the pads 100. The bus bars 110 may serve, for example, as power supplies or grounds, and it is preferred that one bus bar 110 serve one function, such as a power supply, and the second bus bar 110 serve another function, such as a ground.

The silicon chip 50 has bonding pads 120 located generally in the central area of silicon chip 50. The bonding pads 120 are connected to routing strips 82 and bus bars 110 by wire

bonding 80. Even though Figure 1 depicts printed circuit board 70 as having a single layer, the printed circuit board 70 can have a number of layers, depending on the number of conduits and vias that are needed for electrically connecting the bonding pads 120 with the pads 100. It should be understood by one skilled in the art that printed circuit board 70 may consist of a single layer or may be a multi-layered board having an alternate number of layers.

The above described components and their constructions and interrelation provide an assembly that is encapsulated as described below. The term "assembly" refers to the assembled components prior to encapsulation. The assembly consists of printed circuit board 70, adhered silicon chip 50 and wire bonding 80. The printed circuit board 70 has a top opening 86 with routing strips 82 and bus bars 110 extending into the top opening 86. Disposed on pads 100 are solder balls 150.

The wire bonding 80 process begins before silicon chip 50 has been adhered to printed circuit board 70. Silicon chip 50 and printed circuit board 70 are then positioned on a heated pedestal to raise the temperature of the combination to a point between 100°-300°C. A gold wire having a diameter typically ranging from 0.7 mil. to 1.3 mil. is strung through a heated

capillary where the temperature may range between 200°-500°C. A soldering ball is created at the end of the wire using either a flame or a spark technique. The soldering ball is then brought to bonding pad 120 on the silicon chip 50 and a combination of compression force and ultrasonic energy are used to create the desired metallurgical bond. Using this "stitch" technique significantly reduces the cross-section of the wire at that point. A loop is created in the wire bonding 80 above the bond that has just been achieved, and the wire bonding 80 is routed to the desired connection on the printed circuit board 70 such as routing strip 82 or bus bar 110. The wire bonding 80 is clamped and the capillary raised, such that the wire bonding 80 will break free at the outer edge of the bond. This process is repeated until all the bonding pads 120 that require electrical connection on the silicon chip 50 are electrically connected to printed circuit board 70.

Following the assembly of the above-described components, the opening 86 is filled with potting material 90 as represented by the line above opening 86.

The potting material 90 may be a cyanate ester-type resin available from Shin-Etsu Chemical Co., Ltd., such as KMC 184VA and KMC 188VA-4. Other examples of potting materials 90 that

may be used with the present invention include epoxies, polyesters, polyimides, cyanoacrylates, ceramic, silicone and urethane. The potting materials 90 may also contain fillers that affect the coefficient of thermal expansion, as well as the strength and flexibility of the potting material 90. The selection of potting material 90 and fillers will depend on the components used to make the integrated circuit package 30, as will be known to those of skill in the art.

Properties of Typical Potting Resins

	Epoxy	Polyester	Silicone	Urethane
Dielectric constant, D-150				
60 Hz	3.9	4.7	2.7	5.7
10^6 Hz	3.2	---	2.7	3.4
Dissipation factor, D-150				
60 Hz	0.04	0.017	0.001	0.123
10^6 Hz	0.03	---	0.001	0.03
Dielectric strength, D-149; V/mil	450	325	550	400
Volume resistivity, D-257; $\Omega \cdot cm$	10^{15}	10^{14}	10^{15}	10^{13}
Arc resistance, D-495; seconds	150	135	120	180
Specific gravity, D-792	1.15	1.2	1.05	1.0
Water absorption, D-570; % 24 h	0.15	0.3	0.12	0.4
Heat deflection temperature, D-648; at 264 lb/in^2, °F	380	260	< 70	< 70
Tensile strength, D-638; lb/in^2	9000	10,000	1000	2000
Impact strength (Izod), D-256; ft · lb/in	0.5	0.3	No break	No break
Coefficient of thermal expansion, D-969; 10^{-5}/°F	5.5	7.5	4.0	15
Thermal conductivity, C-177; Btu · in/($h \cdot ft^2 \cdot$°F)	1.7	1.7	1.5	1.5
Linear shrinkage; %	0.3	3.0	0.4	2.0
Elongation, D-638; %	3	3	175	300

The solder balls 150 used with the present invention may be attached to the pads 100 using conventional solder reflow systems. For example, a vapor phase solder reflow system may be used, which condenses vapor to surround the integrated circuit

package 30 and the printed circuit board 70 with a cloud of steam. A liquid, such as a nonchlorinated (non CFC) fluorocarbon is first heated with enough energy to form a vapor and to sustain a vapor cloud. When the integrated circuit package 30 is then passed through the vapor, the vaporized liquid condenses thereon and gives off the latent heat of vaporization. This energy is then transferred to the integrated circuit package 30. As long as the integrated circuit package 30 remains in the vapor, the vapor continues to give off energy at a repeatable fixed rate and temperature, until the integrated circuit package 30 reaches the temperature of the vapor.

The advantage of using a nonchlorinated fluorocarbon is that it is extremely thermally stable, colorless, odorless and nonflammable. In addition, it has a low toxicity, low surface temperature, low boiling point, and low heat of vaporization. Because the fluid form of the non-chlorinated fluorocarbon is inert, it does not react with fluxes or component materials, nor does it absorb oxygen or other gases that cause reactions during the solder reflow. Most commercially available fluorocarbons used for vapor phase reflow are formulated to vaporize at precisely stable reflow temperatures for different solder materials, as will be known to those skilled in the art.

The vaporization temperature will depend on the solder type being used. A brief temperature profile for the non-chlorinated fluorocarbons that are used as vapor fluids is shown below.

Vaporization Temperatures and Solder Types

Fluid Temperature	Solder Type
56, 80, 97, 101, 102°C and 155°C	100 In 37 Sn/38 Pb/25 In
165°C	70 Sn/18 Pn/12 In 70 In/30 Pb
174°C	60 In/40 Pb
190°C	90 In/10 Ag 50 In/50 Pb 63 Sn/37 Pb 70 Sn/30 Pb 60 Sn/40 Pb
215°C and 230°C	60 Sn/40 In 60 Sn/40 Pb 63 Sn/37 Pb 70 Sn/30 Pb 62 Sn/36 Pb/2 Ag
240°C and 253°C	75 Pb/25 In 81 Pb/19 In
260°C and 265°C	96.5 Sn/3.5 Ag

Alternatively, infrared or radiant heated solder reflow may be used. In such a system each component of the soldering system is directly exposed to radiation from a heating element.

Heat from the radiant energy element is absorbed by the different components according to its molecular structure.

Conventional radiant heat systems expose only the outer surfaces of the components to the radiant heat, which may not reach interior areas as efficiently as with vapor saturated heating methods as described above. The present invention, however, is not affected by this typical problem because of the use of solder balls 150 instead of leads. In fact, due to the reduced overall size either method, vapor phase solder reflow or radiant heated solder reflow, may be effectively used with the present invention.

The present invention also solves other problems associated with solder reflow systems. These problems include the creation or failure due to voids, coplanarity, tombstoning, open joints, component cracking, thermal shock and thermal stressing. The present invention solves these problems because it dispenses with the need for electrically connecting soldering leads to the integrated circuit package 30. By using solder balls 150 instead of leads, the problems associated with voids around pad areas or under leads caused by incomplete reflow or poor welding of the soldering surface due to improper flux or badly oxidized surfaces is eliminated. The problems of coplanarity and

tombstoning are also reduced or eliminated using the solder balls 150 because surface tension on both sides of the solder balls 150 is equal.

Open joints are usually caused by problems with coplanarity, while cracking may occur when trapped moisture within an integrated circuit package expands as the device is heated for reflow. The increase in internal pressure, causes the integrated circuit package to split open, usually at one of the corners. The splitting of the package causes wire bonding from the lead frame to the silicon chip to break and in some cases the silicon chips have cracked due to the warpage at the top of the package as the temperature differentials between the top and the bottom of the device cause different rates of expansion.

Using the present invention, the only surface temperature differential that occurs is between the solder ball 150 and the printed circuit board 70, which allows either vapor phase solder reflow or radiant heat solder reflow to be available for producing the present invention. The small size of the solder balls 150, and of the integrated circuit package 30 as a whole, allows for any of the reflow systems to be used with the because the temperature differential between the components is almost

negligible. Furthermore, by selecting an adhesive material 90 having a coefficient of thermal expansion similar, or equal to, the coefficient of thermal expansion of the other components of the integrated circuit package 30, heat reflow effects and problems can be minimized.

Although the board-on-chip layout of integrated circuit package 30 as depicted in Figures 1 and 2 has been described using centralized bonding pads 120, it should be understood by one skilled in the art that the principles of the present invention are applicable to a silicon chip 50 with bonding pads 120 in alternate layouts such as positioned along the sides of the silicon chip 50.

Also, it should be noted by one skilled in the art that pads 100 and bus bars 110 may be located on a single layer of printed circuit board 70. Generally, a layer of insulated tape or coating may be placed on the bus bars 110 to provide for electrical isolation. The advantage of a multi-layer printed circuit board 70, however, is the elimination of the need to insulate the bus bars 110. Additionally, the multi-layer printed circuit board 70 provides a greater process margin for wire bonding.

Furthermore, the method of the present invention takes advantage of the top opening 86 at the center of the printed circuit board 70 for "potting" the wire bonding 80 that connect the silicon chip 50 and the printed circuit board 70 in a single step. By filling the opening 86 with an adhesive material 90, the wire bonding 80 between silicon chip 50 and the printed circuit board 70 are generally protected from the environment and are particularly protected from moisture due to the hermetic nature of the encapsulation.

The method of adhering the silicon chip 50 to the printed circuit board 70 of the present invention provides protection for silicon chip 50 by hermetically sealing silicon chip 50 from the environment. A reduce profile is also achieved by allowing the non-operative or backside of the silicon chip 50 to be exposed. By hermetically protecting the connections between the silicon chip 50 and the printed circuit board 70 at the top opening 86, there is no need to completely encapsulate the entire assembly.

The present invention also reduces the overall number of steps in the assembly of, for example, memory units by streamlining the assembly process not only in reduced number of steps, but also by elimination the curing steps associated with

encapsulating integrated circuit. The present invention further reduces the amount of material used in producing integrated circuit packages 30, thereby saving time, money and the environment.

The problems of coplanarity are eliminated by using solder balls 150 to attach the integrated circuit package 30 to another printed circuit board, such as a mother board, because there are no leads that may bend and there are no deviations from the plane of the motherboard to which the module is being connected.

Additionally, reduced environmental impact is obtained using the method and apparatus of the present invention due to the overall decrease in the size of the integrated circuit package 30.

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

What is claimed is:

1. An integrated circuit package comprising:

a substrate having an opening and first and second surfaces;

a metal layer disposed on said second surface of said substrate;

an adhesive layer disposed on said metal layer opposite said substrate; and

a chip having at least one bonding pad adhered to said adhesive layer, wherein said chip and said substrate are electrically connected.

2. The integrated circuit package as recited in claim 1 further including at least one bus bar being integral with said substrate and extending into said opening, said at least one bus bar electrically connected to at least one of said bonding pads.

3. The integrated circuit package as recited in claim 1 further including at least one pad disposed on said first surface of said substrate.

4. The integrated circuit package as recited in claim 3 further including at least one solder ball located on at least one of said pads disposed on said first surface.

5. The integrated circuit package as recited in claim 4 wherein at least one of said solder balls is electrically connected with at least one of said routing strips.

6. The integrated circuit package as recited in claim 1 wherein said substrate is selected from the group consisting of FR-4, FR-5 and BT resin.

7. The integrated circuit package as recited in claim 1 wherein said metal layer is selected from the group consisting of copper, silver or gold or combinations thereof.

8. An integrated circuit package comprising:

a substrate having an opening and first and second surfaces;

an adhesive layer disposed on said second surface of said substrate;

a metal layer disposed on said adhesive layer opposite said substrate; and

a chip having at least one bonding pad disposed on said metal layer, wherein said chip and said substrate are electrically connected.

9. The integrated circuit package as recited in claim 8 further including at least one bus bar being integral with said substrate and extending into said opening, said at least one bus bar electrically connected to at least one of said bonding pads.

10. The integrated circuit package as recited in claim 8 further including at least one pad disposed on said first surface of said substrate.

11. The integrated circuit package as recited in claim 10 further including at least one solder ball located on at least one of said pads disposed on said first surface.

12. The integrated circuit package as recited in claim 11 wherein at least one of said solder balls is electrically connected with at least one of said routing strips.

13. The integrated circuit package as recited in claim 8 wherein said substrate is selected from the group consisting of FR-4, FR-5 and BT resin.

14. The integrated circuit package as recited in claim 8 wherein said metal layer is selected from the group consisting of copper, silver or gold or combinations thereof.

15. A method for attaching a chip to a substrate comprising the steps of:

obtaining a substrate;

disposing a metal layer on said substrate;

attaching an adhesive layer to a chip; and

contacting said adhesive layer to said metal layer, wherein said metal layer increases the bonding strength between the chip and the substrate.

16. The method as recited in claim 15 wherein the step of contacting said adhesive layer to said metal layer further includes the steps of applying heat to said adhesive and metal layers.

17. The method as recited in claim 16 wherein the step of applying heat to the chip is further defined as applying heat at a temperature between about 200° C and 250° C.

18. The method as recited in claim 15 further comprising the step of applying force between said adhesive layer and said metal layer.

19. The method as recited in claim 18 wherein the step of applying a force is further defined as applying a force to said chip of between about 150 and 200 grams.

20. The method as recited in claim 18 wherein the step of applying force is further defined as applying force for a period of between about 2 and 10 seconds.