MULTI-LEVEL GATE SONOS FLASH MEMORY DEVICE WITH HIGH VOLTAGE OXIDE AND METHOD FOR THE FABRICATION THEREOF

ABSTRACT

A method for manufacturing an integrated circuit structure includes providing a semiconductor substrate and forming a gate dielectric layer over the semiconductor substrate. The gate dielectric layer is formed in a plurality of thicknesses in a plurality of devices regions over the semiconductor substrate. A second dielectric layer is formed over at least one of the devices regions. A third dielectric layer is formed over at least a portion of the second dielectric layer. Ion traps are then selectively implanted in portions of the second dielectric layer.

Figure 8