FRAMES LOCKING METHOD FOR PACKAGING SEMICONDUCTOR CHIP

ABSTRACT OF THE DISCLOSURE

The present invention is a mechanism for packaging semiconductor chip which provides ease of assembling and high positioning precision with improved mechanical, electrical and thermal performance. The present invention adopts a die pad frame for supporting the semiconductor chip and a separate lead frame for connection to center part of the semiconductor chip. The semiconductor chip is fixed on the die pad using silver paste, the lead frame conductors are then placed on top of the chip, and the lead frame and the die pad frame containing the chip are assembled with the positioning protrusions of the die pad frame locked and secured by the positioning openings of the lead frame. Subsequently the bonding terminals on the chip are connected to the lead conductors with short gold wires. The frames locking method does not require high precision positioning machines, thereby reducing the assembly cost. The packaged chip contains, from bottom to top, a die pad, the semiconductor chip, a wafer coating, multiple lead conductors and encapsulating material. Since the conductors are placed on top of the semiconductor chip, the positions of the bonding terminals of the chip can be freely designed, and the heat generated by the chip can be dissipated through the conductors more effectively. In addition, because of the adoption of the die pad, the mechanical strength of the packaged chip is improved, while the die pad also helps dissipate the heat generated by the chip.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)