

REPLACEMENT SHEET

1. A universal flash storage (UFS) system comprising:
 - a doorbell register having a number of bits corresponding to a UFS transfer protocol (UTP) Transfer Request List (UTRL);
 - a completion notification register having a same number of bits; and
 - a control system operatively coupled to the doorbell register and the completion notification register and configured to:
 - set a doorbell bit in the doorbell register for a send request start;
 - set a completion bit in the completion notification register on transfer request completion; and
 - clear the doorbell bit on the transfer request completion.
2. The UFS system of claim 1, wherein the control system is further configured to issue a transfer request to a device.
3. The UFS system of claim 2, wherein the send request start is associated with the transfer request.
4. The UFS system of claim 1, further comprising a communication interface configured to couple a host to a device.
5. The UFS system of claim 2, wherein the control system is further configured to clear the completion bit after processing completion of the transfer request.
6. The UFS system of claim 5, wherein the control system is further configured to reuse a slot associated with the completion bit after clearing the completion bit.
7. The UFS system of claim 2, wherein the transfer request includes a write command to write data to the device.
8. The UFS system of claim 2, wherein the transfer request includes a read command to read data from the device.

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9. The UFS system of claim 1 integrated into a device selected from the group consisting of a set top box, an entertainment unit, a navigation device, a communications device, a fixed location data unit, a mobile location data unit, a mobile phone, a cellular phone, a computer, a portable computer, a desktop computer, a personal digital assistant (PDA), a monitor, a computer monitor, a television, a tuner, a radio, a satellite radio, a music player, a digital music player, a portable music player, a digital video player, a video player, a digital video disc (DVD) player, and a portable digital video player.

10. A memory system comprising:
a doorbell register having a number of bits;
a completion register having a same number of bits; and
a control system operatively coupled to the doorbell register and the completion register and configured to:
set a doorbell bit in the doorbell register for a send request start;
set a completion bit in the completion register on transfer request completion; and
clear the doorbell bit on the transfer request completion.

11. A method of controlling a memory system, comprising:
generating a transfer request in a host;
setting a bit in a doorbell register in the host identifying the transfer request;
passing the transfer request to a device through a communication interface;
completing a transfer associated with the transfer request;
clearing the bit in the doorbell register; and
setting a completion bit in a completion register.

12. The method of claim 11, wherein generating the transfer request comprises generating a read command to read data from the device.

13. The method of claim 11, wherein generating the transfer request comprises generating a write command to write data to the device.

14. The method of claim 11, further comprising starting the transfer.

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15. The method of claim 11, further comprising handling interrupts to the transfer request without need for a software lock.
16. The method of claim 11, further comprising receiving an interrupt generated by a second transfer request.
17. The method of claim 11, further comprising clearing the completion bit after processing completion of the transfer request.
18. The method of claim 17, further comprising reusing a slot associated with the completion bit after clearing the completion bit.
19. An embedded Multi-Media Controller (eMMC) memory system comprising:
 - a doorbell register having a number of bits corresponding to an eMMC Task Descriptor List (TDL);
 - a completion notification register having a same number of bits; and
 - a control system operatively coupled to the doorbell register and the completion notification register and configured to:
 - set a doorbell bit in the doorbell register for a send request start;
 - set a completion bit in the completion notification register on transfer request completion; and
 - clear the doorbell bit on the transfer request completion.
20. The eMMC memory system of claim 19, wherein the control system is further configured to issue a transfer request to a device.
21. The eMMC memory system of claim 20, wherein the send request start is associated with the transfer request.
22. The eMMC memory system of claim 19, further comprising a communication interface configured to couple a host to a device.

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23. The eMMC memory system of claim 20, wherein the control system is further configured to clear the completion bit after processing completion of the transfer request.

24. The eMMC memory system of claim 23, wherein the control system is further configured to reuse a slot associated with the completion bit after clearing the completion bit.

25. The eMMC memory system of claim 20, wherein the transfer request includes a write command to write data to the device.

26. The eMMC memory system of claim 20, wherein the transfer request includes a read command to read data from the device.

CLAIMS

1. A universal flash storage (UFS) system comprising:
 - a doorbell register having a number of bits corresponding to a UFS transfer protocol (UTP) Transfer Request List (UTRL);
 - a completion notification register having a same number of bits; and
 - a control system operatively coupled to the doorbell register and the completion notification register and configured to:
 - set a doorbell bit in the doorbell register for a send request start;
 - set a completion bit in the completion notification register on transfer request completion; and
 - clear the doorbell bit on transfer request completion.
2. The UFS system of claim 1, wherein the control system is further configured to issue a transfer request to a device.
3. The UFS system of claim 2, wherein the send request start is associated with the transfer request.
4. The UFS system of claim 1, further comprising a communication interface configured to couple a host to a device.
5. The UFS system of claim 2, wherein the control system is further configured to clear the completion bit after processing completion of the transfer request.
6. The UFS system of claim 5, wherein the control system is further configured to reuse a slot associated with the completion bit after clearing the completion bit.
7. The UFS system of claim 2, wherein the transfer request includes a write command to write data to the device.

8. The UFS system of claim 2, wherein the transfer request includes a read command to read data from the device.

9. The UFS system of claim 1 integrated into a device selected from the group consisting of a set top box, an entertainment unit, a navigation device, a communications device, a fixed location data unit, a mobile location data unit, a mobile phone, a cellular phone, a computer, a portable computer, a desktop computer, a personal digital assistant (PDA), a monitor, a computer monitor, a television, a tuner, a radio, a satellite radio, a music player, a digital music player, a portable music player, a digital video player, a video player, a digital video disc (DVD) player, and a portable digital video player.

10. A memory system comprising:

- a doorbell register having a number of bits;

- a completion register having a same number of bits; and

- a control system operatively coupled to the doorbell register and the completion register and configured to:

 - set a doorbell bit in the doorbell register for a send request start;

 - set a completion bit in the completion register on transfer request completion; and

 - clear the doorbell bit on transfer request completion.

11. A method of controlling a memory system, comprising:

- generating a transfer request in a host;

- setting a bit in a doorbell register in the host identifying the transfer request;

- passing the transfer request to a device through a communication interface;

- completing a transfer associated with the transfer request;

- clearing the bit in the doorbell register; and

- setting a completion bit in a completion register.

12. The method of claim 11, wherein generating the transfer request comprises generating a read command to read data from the device.

13. The method of claim 11, wherein generating the transfer request comprises generating a write command to write data to the device.

14. The method of claim 11, further comprising starting the transfer.

15. The method of claim 11, further comprising handling interrupts to the transfer request without need for a software lock.

16. The method of claim 11, further comprising receiving an interrupt generated by a second transfer request.

17. The method of claim 11, further comprising clearing the completion bit after processing completion of the transfer request.

18. The method of claim 17, further comprising reusing a slot associated with the completion bit after clearing the completion bit.

19. An embedded Multi-Media Controller (eMMC) memory system comprising:

- a doorbell register having a number of bits corresponding to an eMMC Task Descriptor List (TDL);

- a completion notification register having a same number of bits; and

- a control system operatively coupled to the doorbell register and the completion notification register and configured to:

- set a doorbell bit in the doorbell register for a send request start;

set a completion bit in the completion notification register on transfer request completion; and
clear the doorbell bit on transfer request completion.

20. The eMMC memory system of claim **19**, wherein the control system is further configured to issue a transfer request to a device.

21. The eMMC memory system of claim **20**, wherein the send request start is associated with the transfer request.

22. The eMMC memory system of claim **19**, further comprising a communication interface configured to couple a host to a device.

23. The eMMC memory system of claim **20**, wherein the control system is further configured to clear the completion bit after processing completion of the transfer request.

24. The eMMC memory system of claim **23**, wherein the control system is further configured to reuse a slot associated with the completion bit after clearing the completion bit.

25. The eMMC memory system of claim **20**, wherein the transfer request includes a write command to write data to the device.

26. The eMMC memory system of claim **20**, wherein the transfer request includes a read command to read data from the device.