I Claim:

1. A heating plate for a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the heating plate comprising:

an electrically insulating layer;

planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater element made of an insulator-conductor composite, the planar heater zones laterally distributed across the electrically insulating layer and operable to tune a spatial temperature profile on the semiconductor substrate;

power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones;

power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones.

2. The heating plate of Claim 1, wherein the insulator-conductor composite comprises one or more insulator materials selected from the group consisting of Al_2O_3, SiO_2, Y_2O_3, Si_3N_4 and AlN, and one or more conductor materials selected from the group consisting of Al, Cu, Mo, W, Au, Ag, Pt, Pd, C, $MoSi_2$, WC and SiC.

3. The heating plate of Claim 2, wherein the insulator-conductor composite comprises up to 30 wt% of Al_2O_3 and balance of W.

4. The heating plate of Claim 1, wherein the planar heater zones are sized such that:

(a) each planar heater zone is not larger than four device dies being manufactured on the semiconductor substrate,

(b) each planar heater zone is not larger than two device dies being manufactured on the semiconductor substrate,

(c) each planar heater zone is not larger than one device die being manufactured on the semiconductor substrate, or

(d) each planar heater zone is scaled with sizes of device dies on the semiconductor substrate and the overall size of the semiconductor substrate.

5. The heating plate of Claim 1, wherein the planar heater zones are sized such that:

(a) each planar heater zone is 0.1 to 1 cm^2,

(b) each planar heater zone is 1 to 3 cm^2,

(c) each planar heater zone is 3 to 15 cm^2, or

(d) each planar heater zone is 15 to 100 cm^2.

6. The heating plate of Claim 1, wherein the heating plate includes 100 to 1000 planar heater zones wherein each heater element has a serpentine shape.

7. The heating plate of Claim 1, wherein the electrically insulating layer comprises a polymer material, a ceramic material, a fiberglass composite, or a combination thereof.

8. The heating plate of Claim 1, wherein the total number of the power supply lines and the power return lines is equal to or less than the total number of the planar heater zones.

9. The heating plate of Claim 1, wherein a total area of the planar heater zones is from 50% to 99% of an upper surface of the heating plate.

10. The heating plate of Claim 1, wherein the planar heater zones are arranged in a rectangular grid, hexagonal grid or concentric rings; and the planar heater zones are separated from each other by gaps at least 1 millimeter in width and at most 10 millimeters in width.

11. A substrate support assembly comprising:

an electrostatic chuck (ESC) including at least one electrostatic clamping electrode configured to electrostatically clamp a semiconductor substrate on the substrate support assembly;

the heating plate of Claim 1; and

a cooling plate attached to a lower side of the heating plate by a thermal barrier layer.

12. The substrate support assembly of Claim 11, further comprising at least one primary heater layer arranged above or below the planar heater zones of the heating plate, wherein the primary heater layer is electrically insulated from the planar heater zones, the power supply lines, and the power return lines of the heating plate; the primary heater layer includes at least one heater which provides mean temperature control of the semiconductor substrate; and the planar heater zones provide radial and azimuthal temperature profile control of the semiconductor substrate, during processing thereof.

13. The substrate support assembly of Claim 12, wherein the primary heater layer includes two or more primary heaters powered with at least 100 W and the planar heater zones are powered with under 10 W/cm^2.

14. A method of making the heating plate of Claim 1, the method comprising: mixing powders of an insulator and a conductor with a liquid (e.g. methanol, ethanol, acetone, isopropyl alcohol, water, mineral oil) into a slurry, screen printing the slurry on the electrically insulating layer and sintering the slurry.

15. The method of Claim 14, wherein the liquid is selected from the group consisting of methanol, ethanol, acetone, isopropyl alcohol, water, mineral oil and a mixture thereof.

16. The method of Claim 14, wherein the powders have particle sizes from 0.2 to 20 microns.

17. A method for manufacturing the heating plate of Claim 1, comprising:

pressing a mixture of ceramic powder, binder and liquid into sheets;

drying the sheets;

forming vias in the sheets by punching holes therein;

forming the power supply lines and power return lines on the sheets;

forming the heater elements by screen printing or spraying a slurry of insulator and conductor powders;

aligning the sheets;

bonding the sheets together by sintering to form the electrically insulating layer;

filling the vias with a slurry of conducting powder.

18. The method of Claim 17, wherein the power supply lines and power return lines are formed by screen printing a slurry of conducting powder, pressing a precut metal foil, or spraying a slurry of conducting powder.

19. A method for plasma processing semiconductor substrates in a plasma processing chamber containing the substrate support assembly of Claim 11, comprising:

(a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support assembly;

(b) determining a temperature profile that compensates for processing conditions affecting critical dimension (CD) uniformity;

(c) heating the semiconductor substrate to conform to the temperature profile using the substrate support assembly;

(d) igniting plasma and processing the semiconductor substrate while controlling the temperature profile by independently controlled heating of the planar heater zones;

(e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.

I claim:

1. A method of making a heating plate comprising planar independently controllable heater zones laterally distributed across an electrically insulating layer configured to form part of a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, each heater zone comprising one or more heater elements made of an insulator-conductor composite, the method comprising: mixing powders of an insulator and a conductor with a liquid into a slurry, and sintering the slurry wherein the total number of the power supply lines and the power return lines is equal to or less than the total number of the planar heater zones.

2. The method of claim 1, wherein the liquid is selected from the group consisting of methanol, ethanol, acetone, isopropyl alcohol, water, mineral oil and a mixture thereof.

3. The method of claim 1, wherein the powders have particle sizes from 0.2 to 10 microns.

4. The method of claim 1, wherein the insulator-conductor composite comprises one or more insulator selected from the group consisting of Al.sub.2O.sub.3, SiO.sub.2, Si.sub.3N.sub.4, AlN and a mixture thereof, and one or more conductor selected from the group consisting of Al, Cu, Mo, W, Au, Ag, Pt, Pd, C, MoSi.sub.2, WC, SiC and a mixture thereof.

5. The method of claim 4, wherein the insulator-conductor composite comprises up to 30 wt % of Al.sub.2O.sub.3 and balance of W.

6. The method of claim 1, wherein the heating plate includes 100 to 400 planar heater zones.

7. The method of claim 1, wherein the electrically insulating layer comprises a polymer material, a ceramic material, a fiberglass composite, or a combination thereof.

8. The method of claim 1, wherein a total area of the planar heater zones is from 50% to 99% of an upper surface of the heating plate.

9. The method of claim 1, wherein the planar heater zones are arranged in a rectangular grid and the planar heater zones are separated from each other by gaps at least 1 millimeter in width and at most 10 millimeters in width.

10. The method of claim 1, further comprising arranging at least one primary heater layer above or below and the planar heater zones of the heating plate, wherein the primary heater layer is electrically insulated from the planar heater zones, the power supply lines, and the power return lines of the heating plate; the primary heater layer includes at least one heater which provides mean temperature control of the semiconductor substrate; the planar heater zones provide radial and azimuthal temperature profile control of the semiconductor

substrate, during processing thereof.

11. The method of claim 10, wherein the primary heater layer includes two or more heaters.

12. A method for manufacturing a heating plate comprising an electrically insulating layer, planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater element made of an insulator-conductor composite, the planar heater zones laterally distributed across the electrically insulating layer, power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones, power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones, comprising: pressing a mixture of ceramic powder, binder and liquid into sheets; drying the sheets; forming vias in the sheets by punching holes therein; forming the power supply lines and power return lines on the sheets; forming heater elements by screen printing or spraying a slurry of insulator and conductor powders; aligning the sheets; bonding the sheets by sintering to form the electrically insulating layer; filling the vias with a slurry of conducting powder.

13. The method of claim 12, wherein the power supply lines and power return lines are formed by screen printing a slurry of conducting powder, pressing a precut metal foil, or spraying a slurry of conducting powder.

14. A method for plasma processing semiconductor substrates in a plasma processing chamber containing a substrate support assembly comprising an electrostatic chuck (ESC) including at least one electrostatic clamping electrode configured to electrostatically clamp a semiconductor substrate on the substrate support assembly, a heating plate comprising an electrically insulating layer, planar heater zones comprising at least first, second, third and fourth planar heater zones, each comprising one or more heater element made of an insulator-conductor composite, the planar heater zones laterally distributed across the electrically insulating layer and operable to tune a spatial temperature profile on the semiconductor substrate, power supply lines comprising at least a first electrically conductive power supply line electrically connected to the first and second planar heater zones and a second electrically conductive power supply line electrically connected to the third and fourth planar heater zones, power return lines comprising at least a first electrically conductive power return line electrically connected to the first and third planar heater zones and a second electrically conductive power return line electrically connected to the second and fourth planar heater zones, and a cooling plate attached to a lower side of the heating plate by a thermal barrier layer, comprising: (a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support assembly; (b) determining a temperature profile that compensates for processing conditions affecting critical dimension (CD) uniformity; (c) heating the semiconductor substrate to

conform to the temperature profile using the substrate support assembly; (d) igniting plasma and processing the semiconductor substrate while controlling the temperature profile by independently controlled heating of the planar heater zones; (e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.