What is claimed is:

1. A semiconductor device comprising:

a substrate including an NMOS region and a PMOS region;

a first transistor in the NMOS region, wherein the first transistor includes a first gate stack and a first source/drain region on at least one side of the first gate stack; and

a second transistor in the PMOS region, wherein the second transistor includes a second gate stack and a second source/drain region on at least one side of the second gate stack,

wherein the first gate stack includes a first high-dielectric constant insulating film, a first gate electrode layer having a first thickness, a second gate electrode layer, a third gate electrode layer, and a first silicon layer which are sequentially laminated,

wherein the first transistor further comprises first gate spacers on both sides of the first gate stack,

wherein the first, second, and third gate electrode layers and the first silicon layer are between the first gate spacers,

wherein the second gate stack includes a second high-dielectric constant insulating film, a fourth gate electrode layer having a second thickness greater than the first thickness, a fifth gate electrode layer, a sixth gate electrode layer, and a second silicon layer which are sequentially laminated, and

wherein the second gate electrode layer and the fifth gate electrode layer includes lanthanum.

2. The semiconductor device of claim 1, wherein sidewalls of the first, second, and third gate electrode layers directly contact the first gate spacers,

wherein the second transistor further comprises second gate spacers on both sides of the second gate stack,

wherein the fourth, fifth, and sixth gate electrode layers and the second silicon layer are between the second gate spacers, and

wherein sidewalls of the fourth, fifth, and sixth gate electrode layers directly contact the second gate spacers.

3. The semiconductor device of claim 1, wherein the fourth gate electrode layer includes a first metal layer, a second metal layer, and a third metal layer that are sequentially laminated, and

wherein the second metal layer includes a material different from a material included in the first metal layer and the third metal layer.

4. The semiconductor device of claim 3, wherein each of the first metal layer and the third metal layer includes titanium or tantalum.

5. The semiconductor device of claim 3, wherein the second metal layer includes aluminum.

6. The semiconductor device of claim 1, wherein the first gate electrode layer is directly on the first high-dielectric constant insulating film, and

the fourth gate electrode layer is directly on the second high-dielectric constant insulating film.

7. The semiconductor device of claim 1, wherein the substrate includes a cell array region and a peripheral region,

wherein the NMOS region and the PMOS region are included in the peripheral region, and

wherein the cell array region includes a buried gate structure.

8. A semiconductor device comprising:

a substrate comprising a cell array region including a buried gate structure, and a peripheral region including a NMOS region and a PMOS region having different conductivity types;

a first transistor in the NMOS region, wherein the first transistor includes a first gate stack, a first source/drain region on at least one side of the first gate stack, and a first channel region below the first gate stack; and

a second transistor in the PMOS region, wherein the first transistor includes a second gate stack, a second source/drain region on at least one side of the second gate stack, and a second channel region below the second gate stack,

wherein the first gate stack includes a first high-dielectric constant insulating film, a first gate electrode layer having a first thickness, a second gate electrode layer, a third gate electrode layer, and a first silicon layer which are sequentially laminated,

wherein the first transistor further comprises first gate spacers on both sides of the first gate stack, and the first, second, and third gate electrode layers and the first silicon layer are between the first gate spacers,

wherein the second gate stack includes a second high-dielectric constant insulating film, a fourth gate electrode layer having a second thickness greater than the first thickness,

a fifth gate electrode layer, a sixth gate electrode layer, and a second silicon layer which are sequentially laminated,

wherein the first channel region and the second channel region include materials different from each other, and

wherein the second gate electrode layer and the fifth gate electrode layer includes lanthanum.

9. The semiconductor device of claim 8, wherein sidewalls of the first, second, and third gate electrode layers directly contact the first gate spacers,

the second transistor further comprises second gate spacers on both sides of the second gate stack,

the fourth, fifth, and sixth gate electrode layers and the second silicon layer are between the second gate spacers, and

sidewalls of the fourth, fifth, and sixth gate electrode layers directly contact the second gate spacers.

10. The semiconductor device of claim 8, wherein the fourth gate electrode layer includes a first metal layer, a second metal layer, and a third metal layer that are sequentially laminated, and

the second metal layer includes a material different from a material included in the first metal layer and the third metal layer.

11. The semiconductor device of claim 10, wherein each of the first metal layer and the third metal layer comprises titanium or tantalum.

12. The semiconductor device of claim 10, wherein the second metal layer includes aluminum.

13. The semiconductor device of claim 8, wherein the buried gate structure includes a buried gate trench, a buried gate insulation film, a buried gate electrode, and a buried gate capping film.

14. The semiconductor device of claim 8, wherein the second channel region includes a material different from the substrate.

15. The semiconductor device of claim 14, wherein the second channel region includes silicon germanium (SiGe).

16. A semiconductor device comprising:

a substrate including an NMOS region and a PMOS region;

a first gate stack on the substrate in the NMOS region;

first gate spacers on both sides of the first gate stack;

a first channel region below the first gate stack;

a second gate stack on the substrate in the PMOS region; and

a second channel region which is below the second gate stack and includes a material different from the first channel region,

wherein the first gate stack includes a first high-dielectric constant insulating film, a first gate electrode layer, a second gate electrode layer, a third gate electrode layer, and a first silicon layer which are sequentially laminated,

wherein the first, second, and third gate electrode layers and the first silicon layer are between the first gate spacers,

wherein the second gate stack includes a second high-dielectric constant insulating film, a fourth gate electrode layer, a fifth gate electrode layer, a sixth gate electrode layer, and a second silicon layer which are sequentially laminated,

wherein the second channel region includes germanium,

wherein the first gate electrode layer and the fourth gate electrode layer include the same metal element,

wherein the second gate electrode layer includes lanthanum, and

wherein the fifth gate electrode layer includes lanthanum or aluminum.

17. The semiconductor device of claim 16, wherein the fourth gate electrode layer includes a first metal layer, a second metal layer, and a third metal layer which are sequentially laminated, and

the second metal layer includes a material different from a material included in the first metal layer and the third metal layer.

18. The semiconductor device of claim 17, wherein the fifth gate electrode layer comprises lanthanum, and the third metal layer comprises aluminum.

19. The semiconductor device of claim 17, wherein the third gate electrode layer includes a fourth metal layer, a fifth metal layer, and a sixth metal layer interposed between the fourth metal layer and the fifth metal layer, and

the sixth metal layer includes a material different from a material included in the fourth metal layer and the fifth metal layer.

20. The semiconductor device of claim 19, wherein the sixth metal layer and the fifth gate electrode layer includes aluminum.