We claim:

1. An electronics (100, 200) including an electrical isolation, the electronics (100, 200) comprising:

a bidirectional isolation circuit (110, 210) separating a first portion (100a, 200a) from a second portion (100b, 200b); and

a bus transceiver switch (120b, 220b) disposed in the second portion (100b, 200b), the bus transceiver switch (120b, 220b) being communicatively coupled to the bidirectional isolation circuit (110, 210);

wherein the bus transceiver switch (120b, 220b) receives from the bidirectional isolation circuit (110, 210) a communication control signal provided by the first portion (100a, 200a).

2. The electronics (100, 200) of claim 1, wherein the bidirectional isolation circuit (110, 210) is comprised of a transformer (112, 212) having a processor terminal (110a, 210a) and a bus terminal (110b, 210b).

3. The electronics (200) of claim 2, wherein the bidirectional isolation circuit (210) further comprises:

a pulse generation circuit (214a) communicatively coupled to the transformer (212), the pulse generation circuit (214a) being configured to:

receive the communication control signal;

generate a pulse signal based on the communication control signal; and

provide the pulse signal to the transformer (212); and

a pulse decode circuit (214b) communicatively coupled to the transformer (212) and configured to receive the pulse signal from the transformer (212) and decode the received pulse signal into the communication control signal received by the bus transceiver switch (220b).

4. The electronics (100) of one of any of the foregoing claims 1 through 3, wherein the bidirectional isolation circuit (110) is further comprised of a control isolation circuit (114) configured to receive the communication control signal from the first portion

(100a) of the electronics (100) and provide the communication control signal to the bus transceiver switch (120b).

5. The electronics (100) of claim 4, wherein the control isolation circuit (114) is comprised of:

a pulse generation circuit (414a) and configured to receive the communication control signal and generate a pulse signal based on the communication control signal;

a transformer (412) communicatively coupled to the pulse generation circuit (414a) and configured to receive the pulse signal from the pulse generation circuit (414a) and provide the pulse signal; and

a pulse decode circuit (414b) communicatively coupled to the transformer (412) and configured to receive the pulse signal provided by the transformer (412) and decode the received pulse signal into the communication control signal received by the bus transceiver switch (120b, 220b).

6. The electronics (100, 200) of one of any of the foregoing claims 1 through 5, further comprising a processor transceiver switch (120a, 220a) disposed in the first portion (100a, 200a) of the electronics (100, 200), the processor transceiver switch (120a, 220a) being configured to be controlled by the communication control signal.

7. The electronics (100, 200) of claim 6, further comprising a processor transceiver circuit (130a, 230a) having a processor transmit terminal (132at, 232at) and a processor receive terminal (134at, 234at), wherein the processor transceiver switch (120a, 220a) is selectively communicatively coupled with the processor transmit terminal (132at, 232at) and the processor receive terminal (134at, 234at).

8. The electronics (100, 200) of claim 7, wherein the processor transceiver circuit (130a, 230a) is comprised of a processor transmit circuit (132a, 232a) and a processor receive circuit (134a, 234a), wherein:

the processor transmit circuit (132a, 232a) is configured to receive a digital communication from a processor (140, 240) in the first portion (100a,

200a) and transmit the received digital communication to the processor transceiver switch (120a, 220a); and

the processor receive circuit (134a, 234a) is configured to receive a digital communication from the processor transceiver switch (120a, 220a) and transmit the received digital communication to the processor (140, 240).

9. The electronics (100, 200) of one of any of the foregoing claims 1 through 8, further comprising a bus transceiver circuit (130b, 230b) having a bus transmit terminal (132bt, 232bt) and a bus receive terminal (134bt, 234bt), wherein the bus transceiver switch (120b, 220b) is selectively communicatively coupled with the bus transmit terminal (132bt, 232bt) and the bus receive terminal (134bt, 234bt).

10. The electronics (100, 200) of claim 9, wherein the bus transceiver circuit (130b, 230b) is comprised of a bus transmit circuit (132b, 232b) and a bus receive circuit (134b, 234b), wherein:

the bus transmit circuit (132b, 232b) is configured to receive a digital communication from the bus transceiver switch (120b, 220b) and transmit the received digital communication to a bus loop (L1, L2); and

the bus receive circuit (134b, 234b) is configured to receive a digital communication from the bus loop (L1, L2) and transmit the received digital communication to the bus transceiver switch (120b, 220b).

11. A method of electrically isolating a portion of an electronics, the method comprising:

receiving at a bidirectional isolation circuit a communication control signal, wherein:

the bidirectional isolation circuit separates a first portion and a second portion of the electronics; and

the communication control signal is provided by the first portion; and

providing with the bidirectional isolation circuit the received communication control signal to a bus transceiver switch disposed in the second portion.

12. The method of claim 11, further comprising providing a transformer in the bidirectional isolation circuit, the transformer having a processor terminal and a second terminal.

13. The method of claim 12, further comprising:

providing and communicatively coupling a pulse generation circuit to the transformer, wherein the pulse generation circuit:

receives the communication control signal from the first portion;

generates a pulse signal based on the communication control signal; and

provides the pulse signal to the transformer; and

providing and communicatively coupling a pulse decode circuit to the transformer, wherein the pulse decode circuit receives the pulse signal from the transformer and decodes the received pulse signal into the communication control signal received by the bus transceiver switch.

14. The method of one of any of the foregoing claims 11 through 13, further comprising:

providing a control isolation circuit;

receiving with the control isolation circuit the communication control signal; and

providing with the control isolation circuit the received communication control signal to the bus transceiver switch disposed in the second portion.

15. The method of claim 14, wherein providing the control isolation circuit comprises:

providing a pulse generation circuit that receives the communication control signal and generates a pulse signal based on the communication control signal;

providing and communicatively coupling a transformer to the pulse generation circuit, wherein the transformer receives the pulse signal from the pulse generation circuit and provides the pulse signal; and

providing and communicatively coupling a pulse decode circuit to the transformer, wherein the pulse decode circuit receives the pulse signal

provided by the transformer and decodes the received pulse signal into the communication control signal received by the bus transceiver switch.

16. The method of one of any of the foregoing claims 11 through 15, further comprising providing and disposing a processor transceiver switch in the first portion and configuring the processor transceiver switch to be controlled by the communication control signal.

17. The method of claim 16, further comprising providing a processor transceiver circuit having a processor transmit terminal and a processor receive terminal and selectively communicatively coupling the processor transceiver switch with the processor transmit terminal and the processor receive terminal.

18. The method of claim 17, wherein providing the processor transceiver circuit comprises providing a processor transmit circuit and a processor receive circuit and the method further comprising:

receiving with the processor transmit circuit a digital communication provided by a processor in the first portion and transmitting with the processor transmit circuit the received digital communication to the processor transceiver switch; and

receiving with the processor receive circuit a digital communication from the processor transceiver switch and transmitting with the processor receive circuit the received digital communication to the processor.

19. The method of one of any of the foregoing claims 11 through 18, further comprising providing a bus transceiver circuit having a bus transmit terminal and a bus receive terminal and selectively communicatively coupling the bus transceiver switch with the bus transmit terminal and the bus receive terminal.

20. The method of claim 19, wherein the providing the bus transceiver circuit comprises providing a bus transmit circuit and a bus receive circuit and further comprising:

receiving with the bus transmit circuit a digital communication from the bus transceiver switch and transmitting the received digital communication to a bus loop; and

receiving with the bus receive circuit a digital communication from the bus loop and transmitting the received digital communication to the bus transceiver switch.