FIG. 1

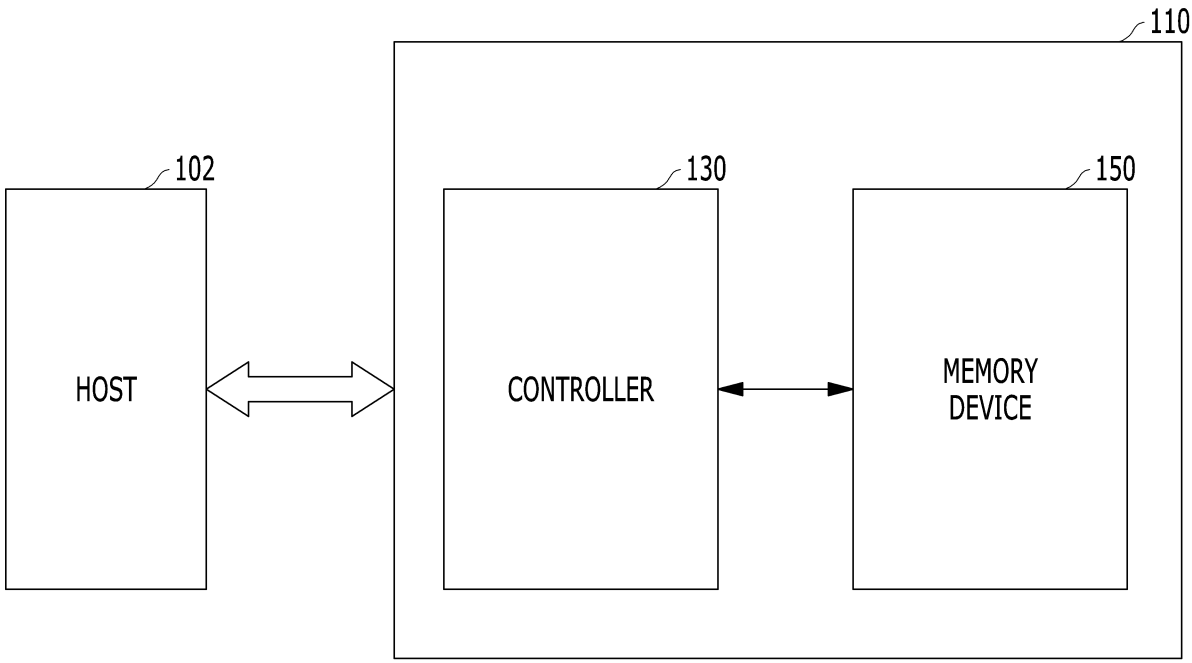


FIG. 2

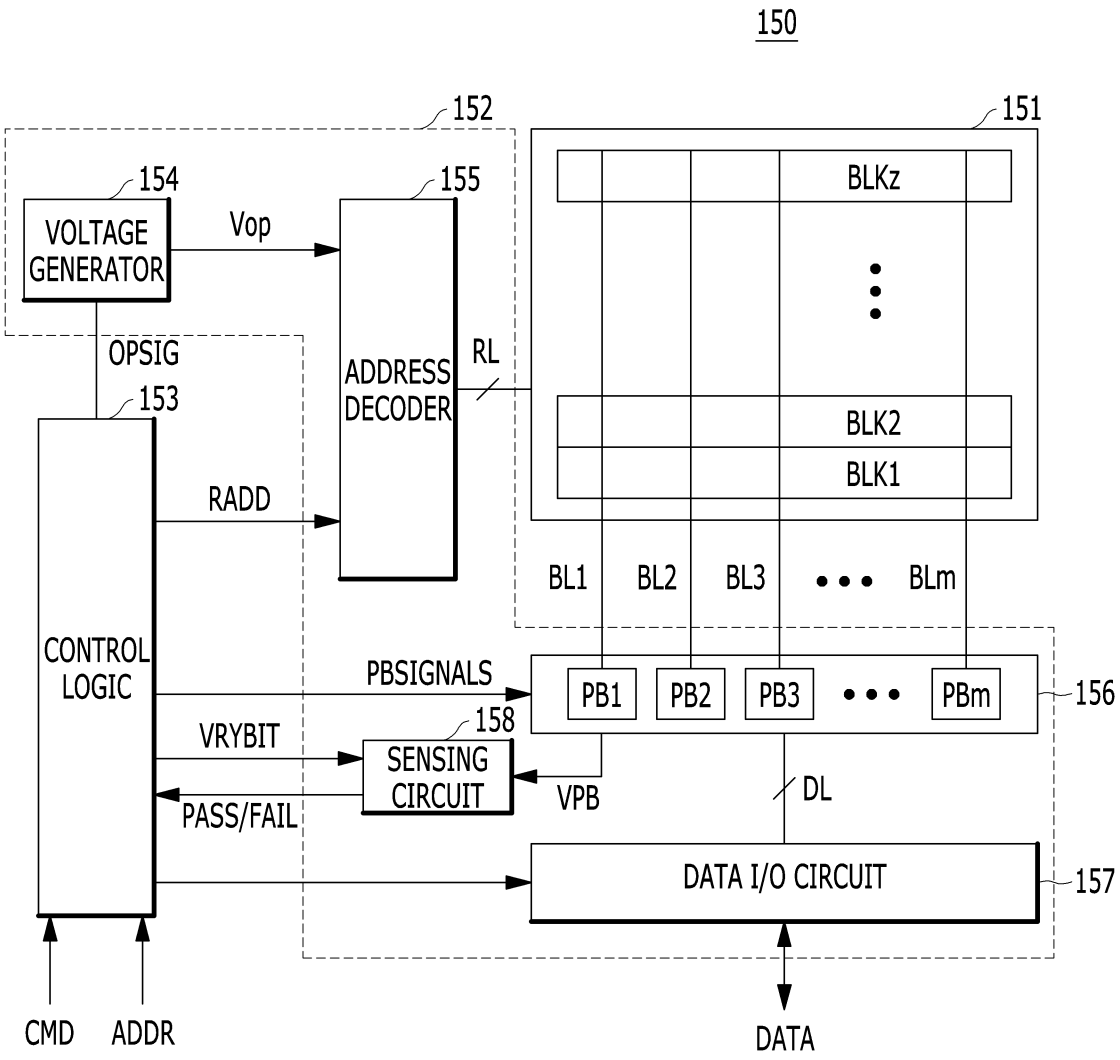

150
152
151
154
155
VOLTAGE GENERATOR
Vop
ADDRESS DECODER
RL
OPSIG
153
BLKz
BLK2
BLK1
RADD
BL1
BL2
BL3
BLm
CONTROL LOGIC
PBSIGNALS
PB1
PB2
PB3
PBm
156
158
VRYBIT
SENSING CIRCUIT
VPB
DL
PASS/FAIL
DATA I/O CIRCUIT
157
CMD
ADDR
DATA

FIG. 3

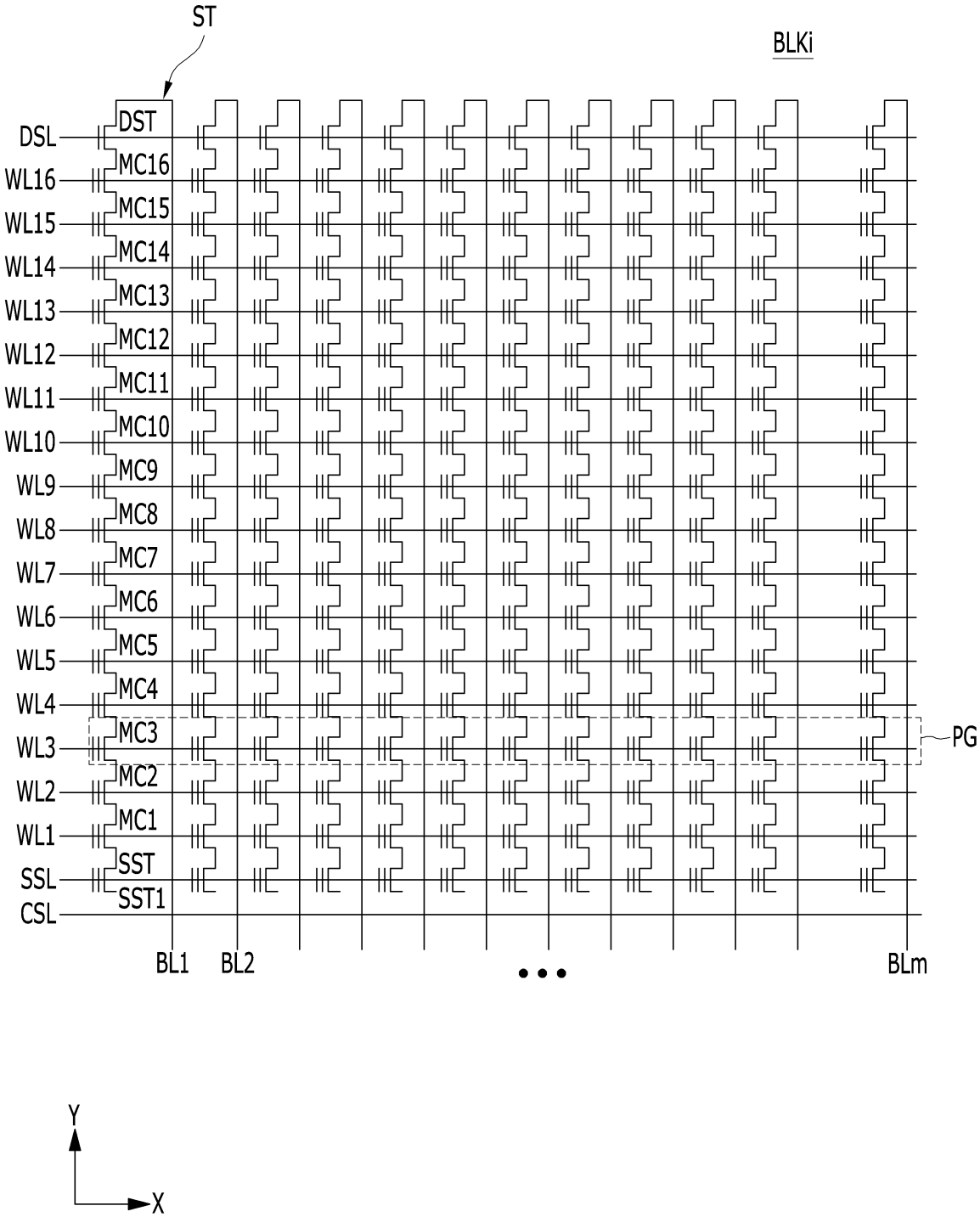

ST
BLKi
DST
DSL
MC16
WL16
MC15
WL15
MC14
WL14
MC13
WL13
MC12
WL12
MC11
WL11
MC10
WL10
MC9
WL9
MC8
WL8
MC7
WL7
MC6
WL6
MC5
WL5
MC4
WL4
MC3
WL3
MC2
WL2
MC1
WL1
SST
SSL
SST1
CSL
PG
BL1
BL2
BLm
Y
X

FIG. 4

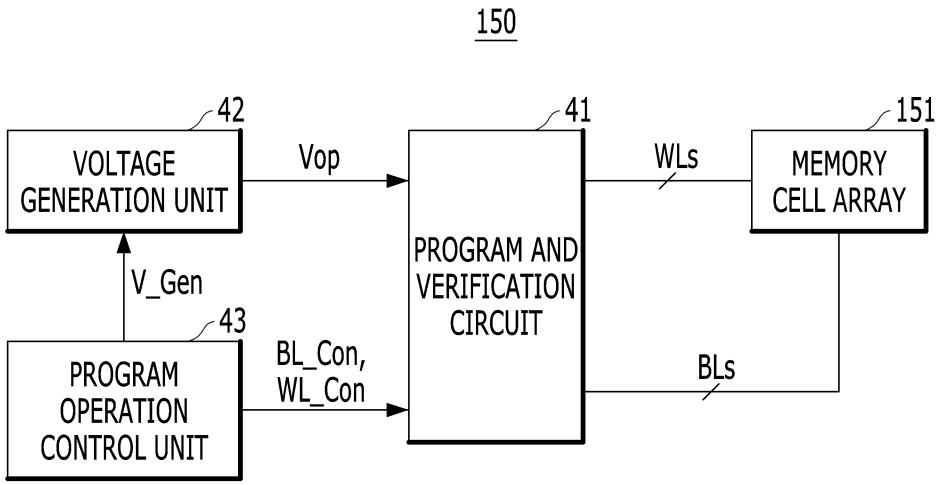

150
42
VOLTAGE GENERATION UNIT
Vop
41
PROGRAM AND VERIFICATION CIRCUIT
WLs
151
MEMORY CELL ARRAY
V_Gen
43
PROGRAM OPERATION CONTROL UNIT
BL_Con, WL_Con
BLs

FIG. 5

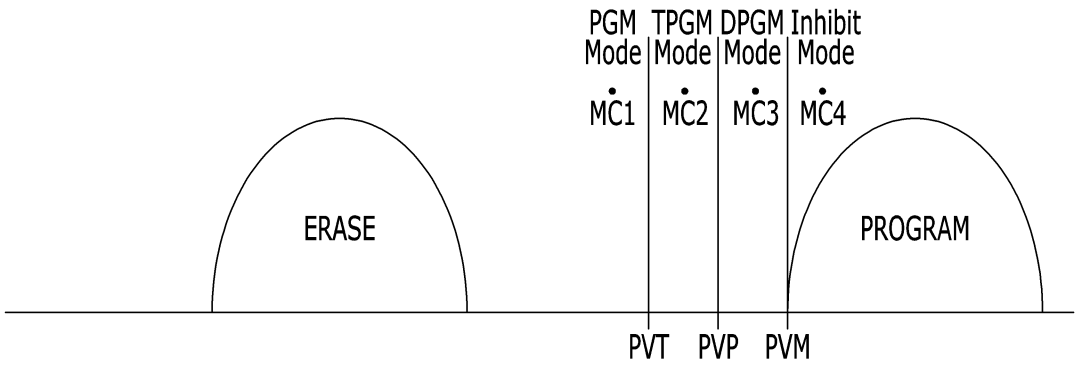

PGM Mode
TPGM Mode
DPGM Mode
Inhibit Mode
MC1
MC2
MC3
MC4
ERASE
PROGRAM
PVT
PVP
PVM

FIG. 6

PVM	PVP	PVT	MODE
ON	ON	ON	PGM
ON	ON	OFF	TPGM
ON	OFF	OFF	DPGM
OFF	OFF	OFF	INHIBIT
OFF	ON	ON	MODE
OFF	OFF	ON	
ON	OFF	ON	
OFF	ON	OFF	

FIG. 7

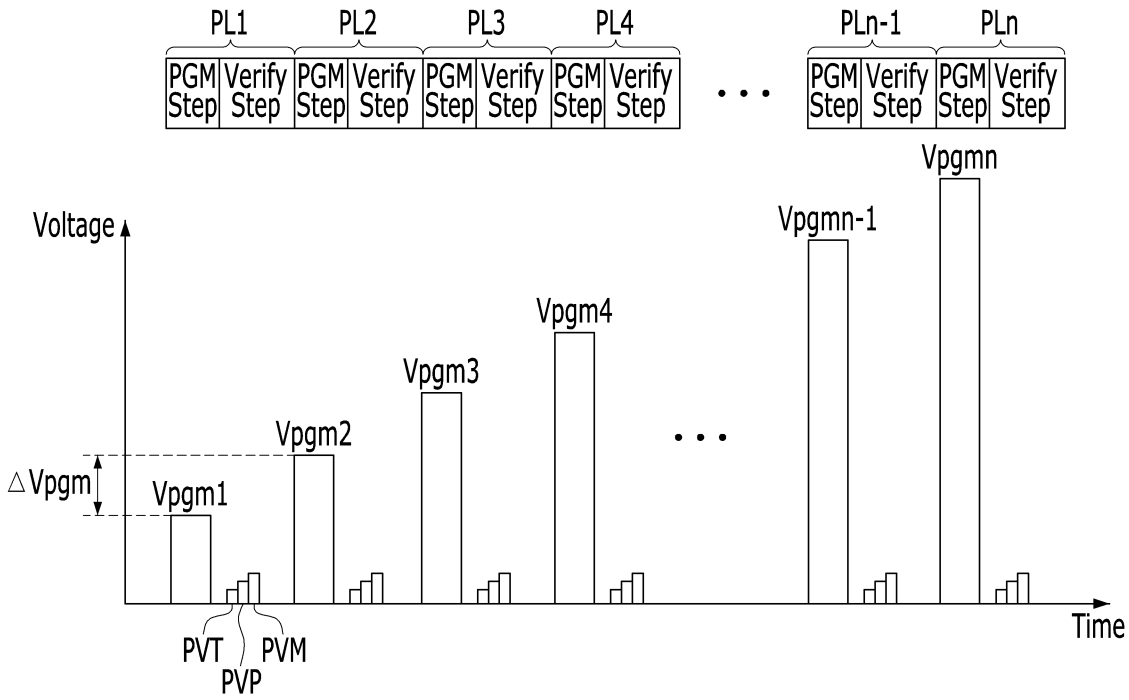

PL1
PL2
PL3
PL4
PLn-1
PLn
PGM Step
Verify Step
Voltage
Vpgm1
Vpgm2
Vpgm3
Vpgm4
Vpgmn-1
Vpgmn
△Vpgm
PVT
PVP
PVM
Time

FIG. 8

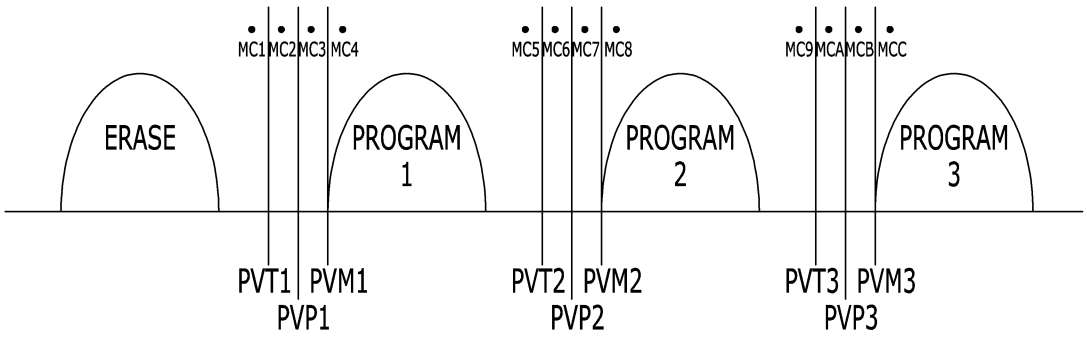

MC1
MC2
MC3
MC4
MC5
MC6
MC7
MC8
MC9
MCA
MCB
MCC
ERASE
PROGRAM 1
PROGRAM 2
PROGRAM 3
PVT1
PVM1
PVP1
PVT2
PVM2
PVP2
PVT3
PVM3
PVP3

FIG. 9

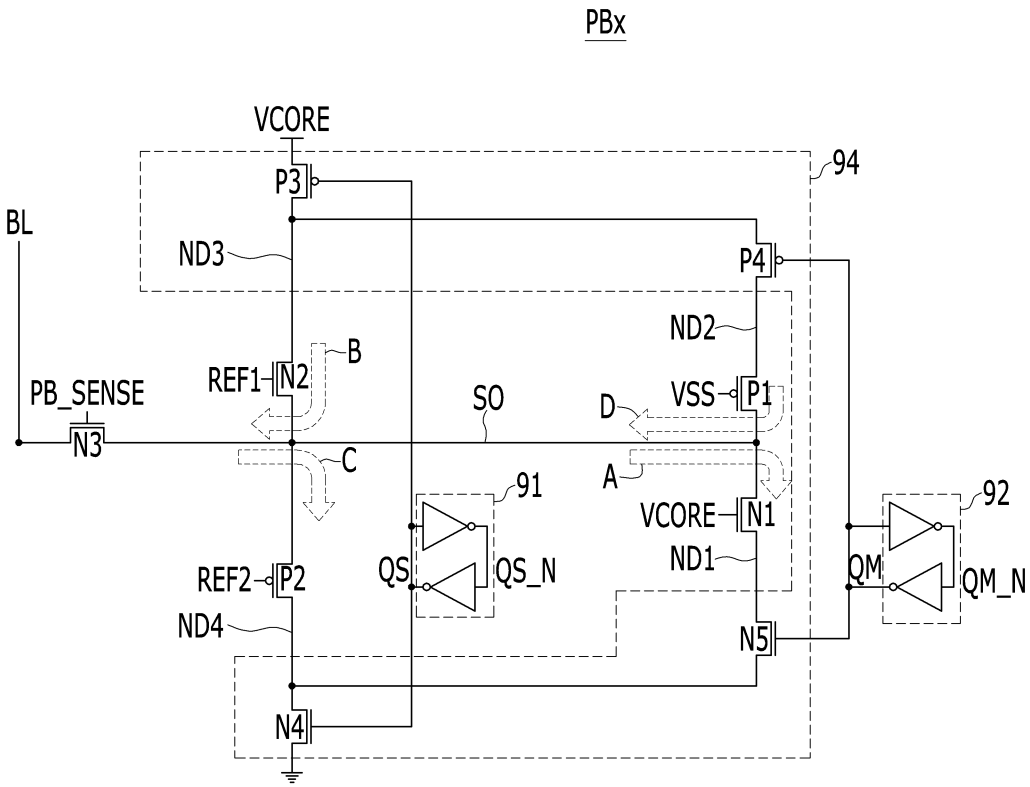

PBx
VCORE
94
P3
BL
ND3
P4
ND2
B
REF1
N2
PB_SENSE
SO
D
VSS
P1
N3
C
A
91
92
VCORE
N1
QS
QS_N
ND1
QM
QM_N
REF2
P2
ND4
N5
N4

FIG. 10

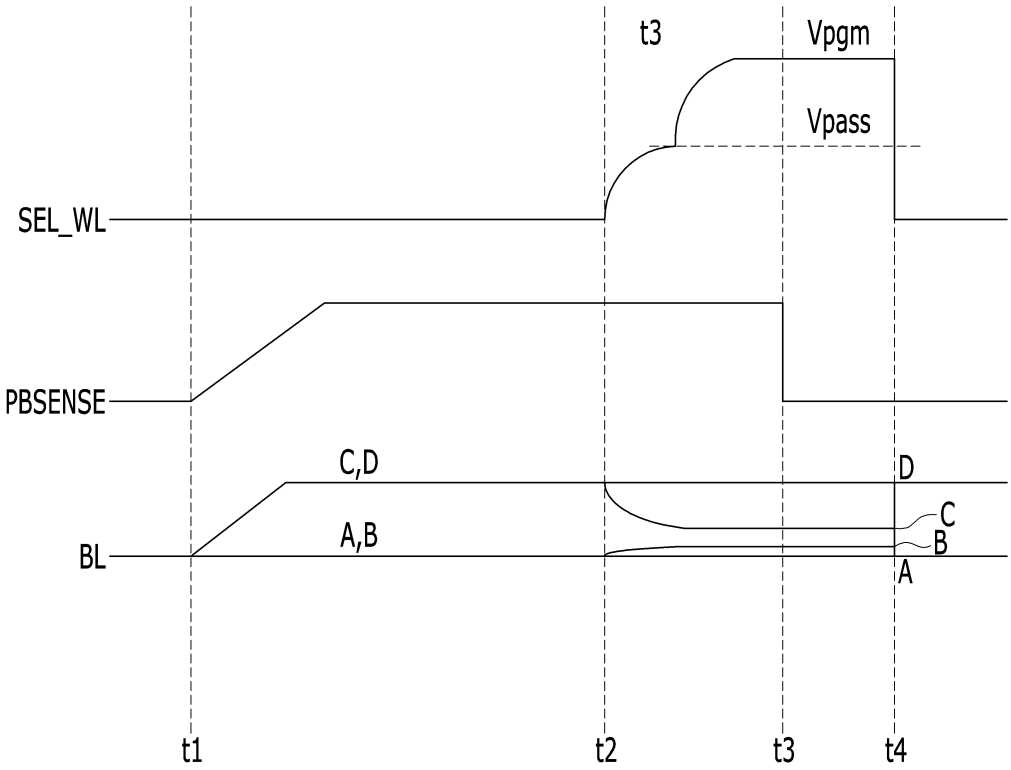


FIG. 11

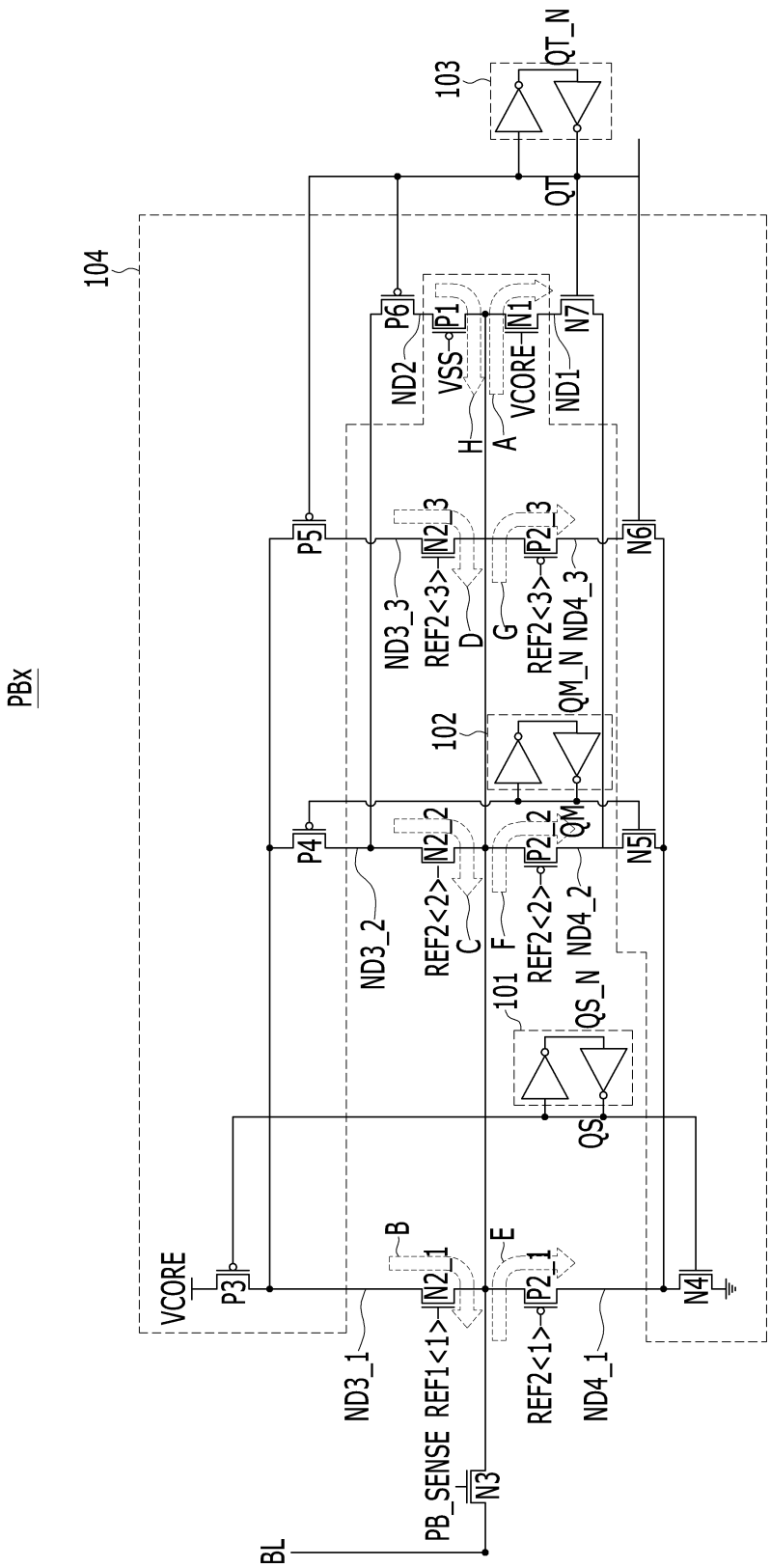

PBx
104
103
QT_N
QT
P6
P1
N1
N7
ND2
VSS
VCORE
ND1
H
A
P5
N2_3
P2_3
N6
ND3_3
REF2<3>
D
G
REF2<3>
ND4_3
QM_N
102
QM
P4
N2_2
P2_2
N5
ND3_2
REF2<2>
C
F
REF2<2>
ND4_2
101
QS_N
QS
VCORE
P3
B
N2_1
E
P2_1
N4
ND3_1
REF1<1>
REF2<1>
ND4_1
PB_SENSE
N3
BL

FIG. 12

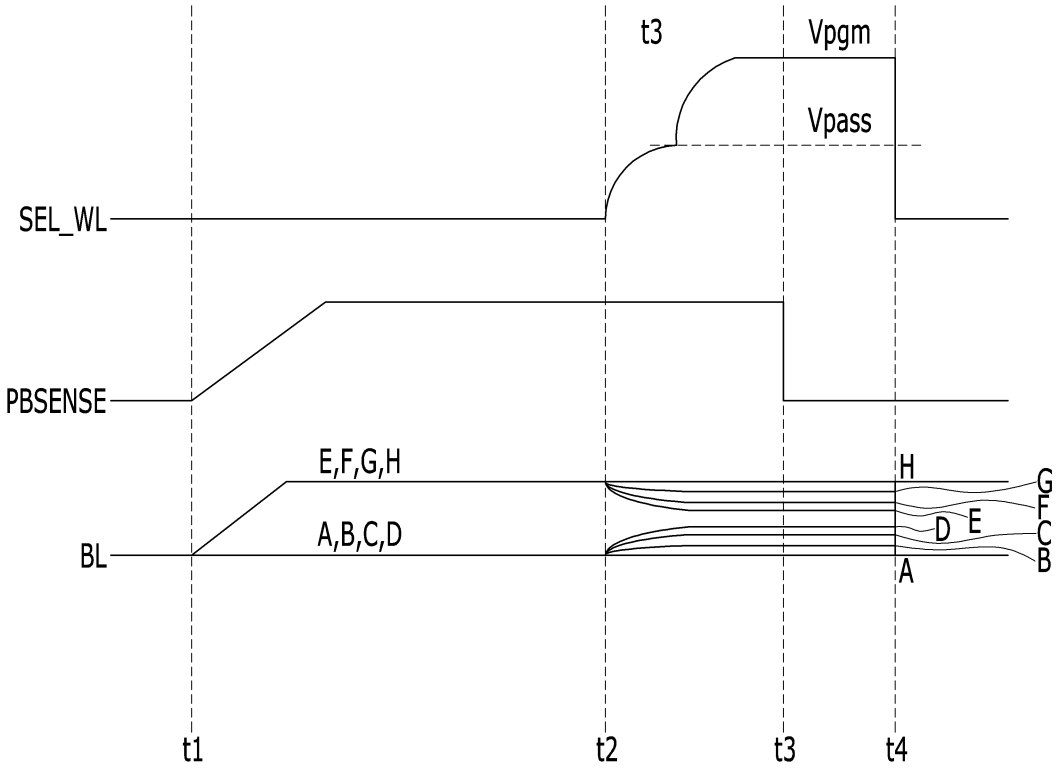


FIG. 13

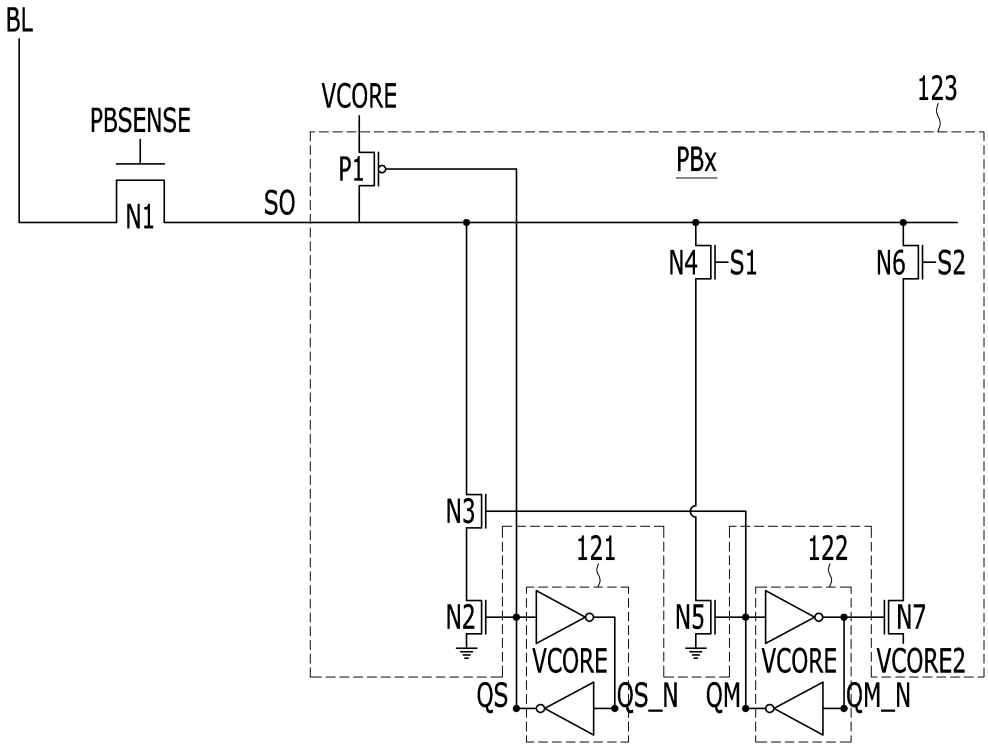

BL
PBSENSE
N1
SO
VCORE
P1
123
PBx
N4
S1
N6
S2
N3
121
122
N2
N5
N7
VCORE
VCORE
VCORE2
QS
QS_N
QM
QM_N

FIG. 14

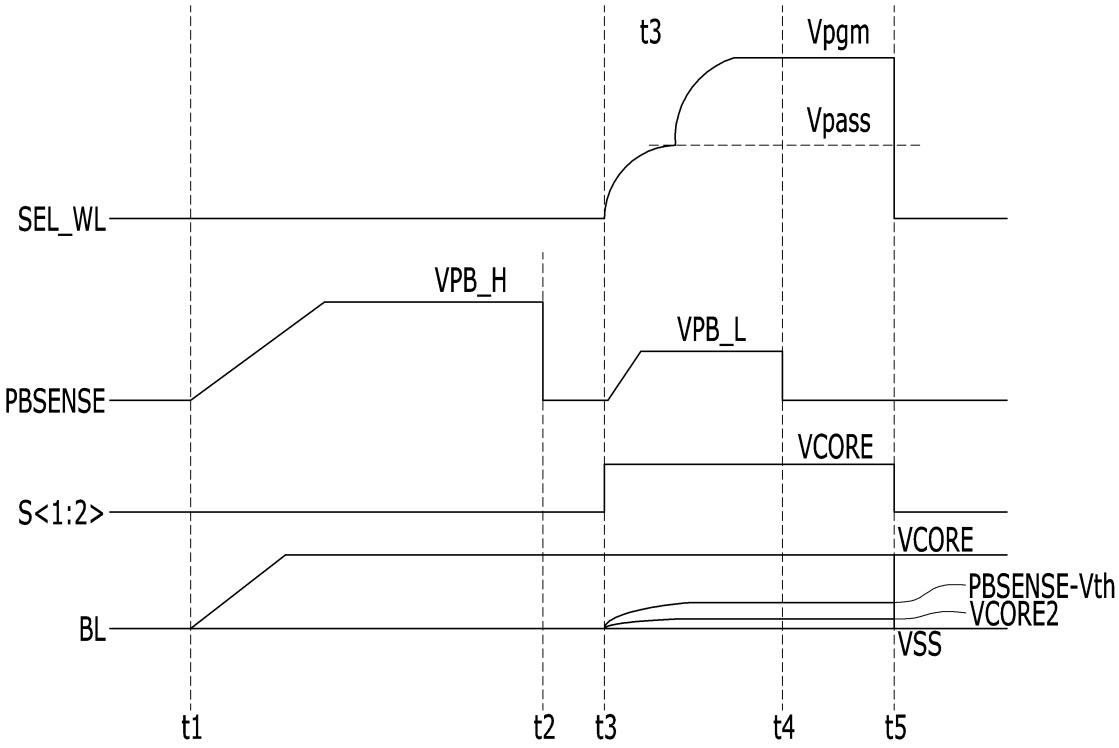

t3
Vpgm
Vpass
SEL_WL
VPB_H
VPB_L
PBSENSE
VCORE
S<1:2>
VCORE
PBSENSE-Vth
VCORE2
BL
VSS
t1
t2
t3
t4
t5

FIG. 15

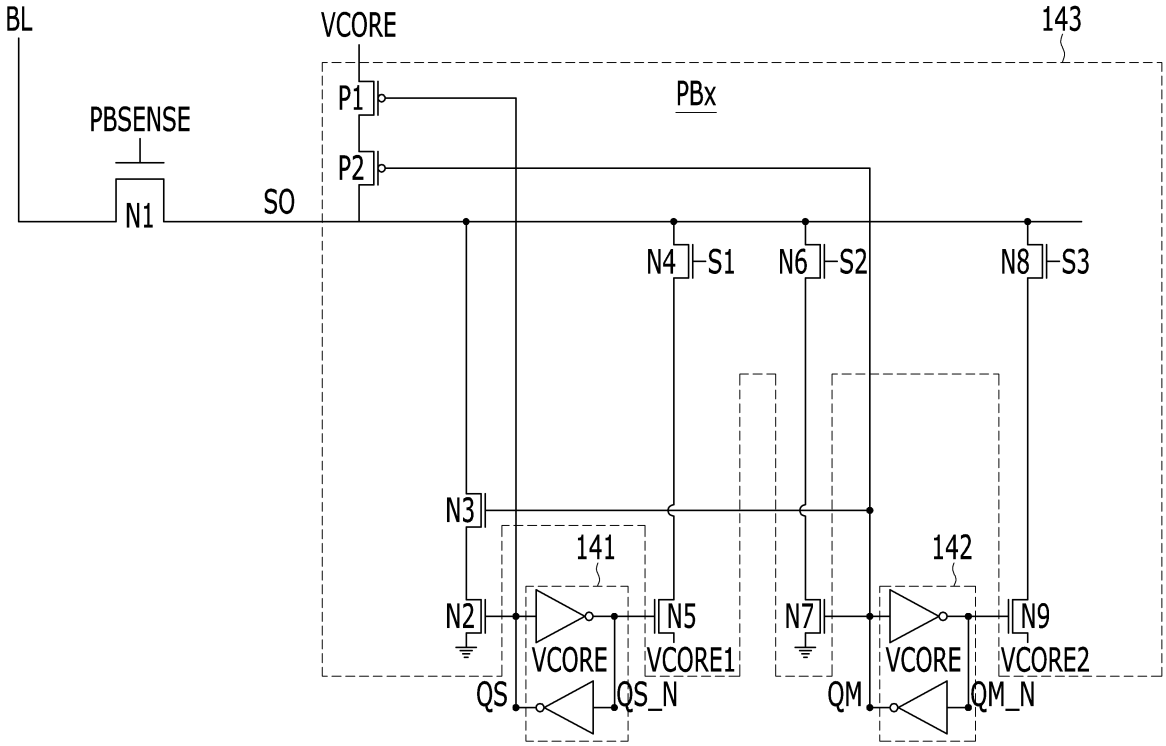
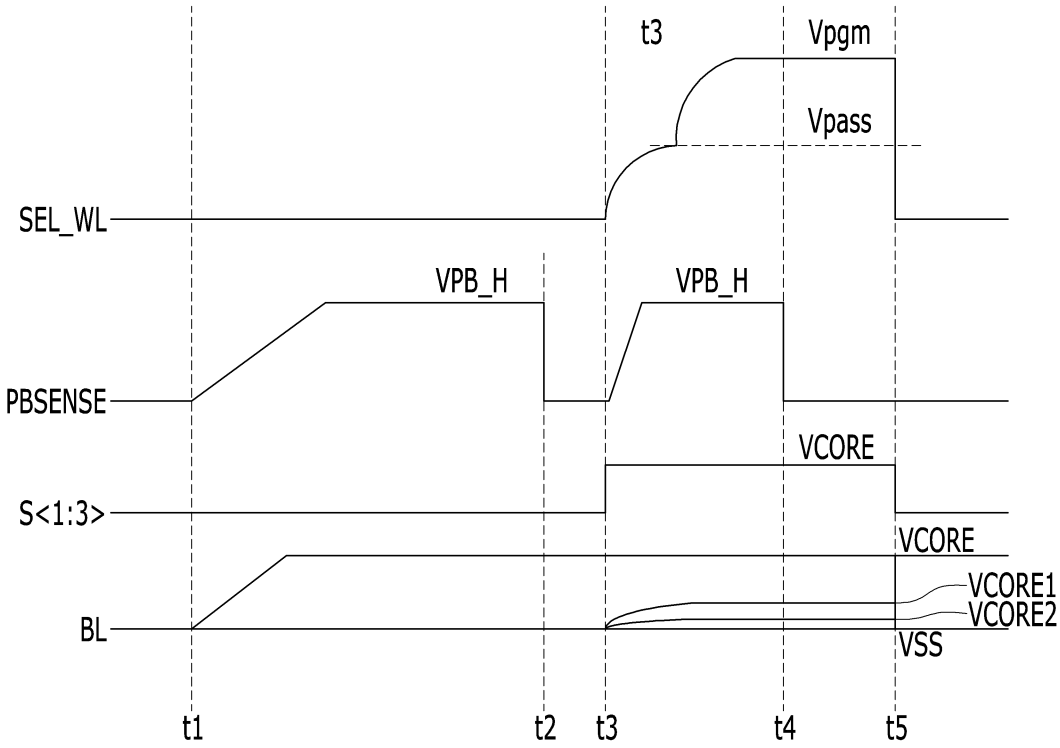

BL
VCORE
143
PBx
P1
P2
PBSENSE
N1
SO
N4
S1
N6
S2
N8
S3
N3
141
142
N2
N5
N7
N9
VCORE
VCORE1
VCORE
VCORE2
QS
QS_N
QM
QM_N

FIG. 16


t3
Vpgm
Vpass
SEL_WL
VPB_H
VPB_H
PBSENSE
VCORE
S<1:3>
VCORE
VCORE1
VCORE2
BL
VSS
t1
t2
t3
t4
t5